ProASIC^{PLUS}™ Family Flash FPGAs

Features and Benefits

High Capacity

- 150,000 to 1 million System Gates
- 36k to 198 kbits of Two-Port SRAM
- 106 to 712 User I/Os

Performance

- 3.3V, 32-bit PCI (up to 50 MHz)
- Internal System Performance up to 350 MHz
- External System Performance up to 150 MHz

Reprogrammable Flash Technology

- 0.22µ 4LM Flash-based CMOS Process
- Live at Power Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design During Power-Down/ Power-Up Cycles

Secure Programming

- The Industry's Most Effective Security Key Prevents Read Back of Programming Bit Stream

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy

- Ultra Fast Local and Long Line Network
- High Speed Very Long Line Network
- High Performance, Low Skew, Splitable Global Network
- 100% Routability and Utilization

I/O

- Schmitt Trigger option on Every Input
- Mixed 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across ProASIC^{PLUS} Family

Unique Clock Conditioning Circuitry

- Two Integrated PLLs (1.5 to 240 MHz Input and Output Ranges)
- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs

- Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- Synchronous and Asynchronous Operation of 24 RAM and FIFO Configurations (Up to 150 MHz)

ProASIC^{PLUS} Product Profile

Device	APA150	APA300	APA450	APA600	APA750	APA1000
Maximum System Gates	150,000	300,000	450,000	600,000	750,000	1,000,000
Maximum Registers	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits	36k	72k	108k	126k	144k	198k
Embedded RAM Blocks (256 X 9)	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2
PLL	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4
Maximum Clocks	32	32	48	56	64	88
Maximum User I/Os	242	304	356	456	642	712
JTAG	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)						
PQFP	208	208	208	208	208	208
PBGA	456	456	456	456	456	456
FBGA	144, 256	144, 256	144, 256	256, 676	676, 896	896, 1152

General Description

The ProASICPLUS family of devices offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASICPLUS family offers a unique clock conditioning circuit based on two on-board phase lock loops (PLLs). The family offers up to 1 million system gates, supported with up to 198 kbits of 2-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power up, unlike SRAM-based FPGAs. No external Boot PROM is required to support device programming. While on-board security mechanisms prevent all access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASICPLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASICPLUS family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22m LVCMOS process with four-layer metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. The result is predictable performance fully compatible with gate arrays.

The ProASICPLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-TilesTM. Each tile can be configured as a flip-flop, latch, or 3-input/1-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a 4-level routing hierarchy.

Embedded 2-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depth and width. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

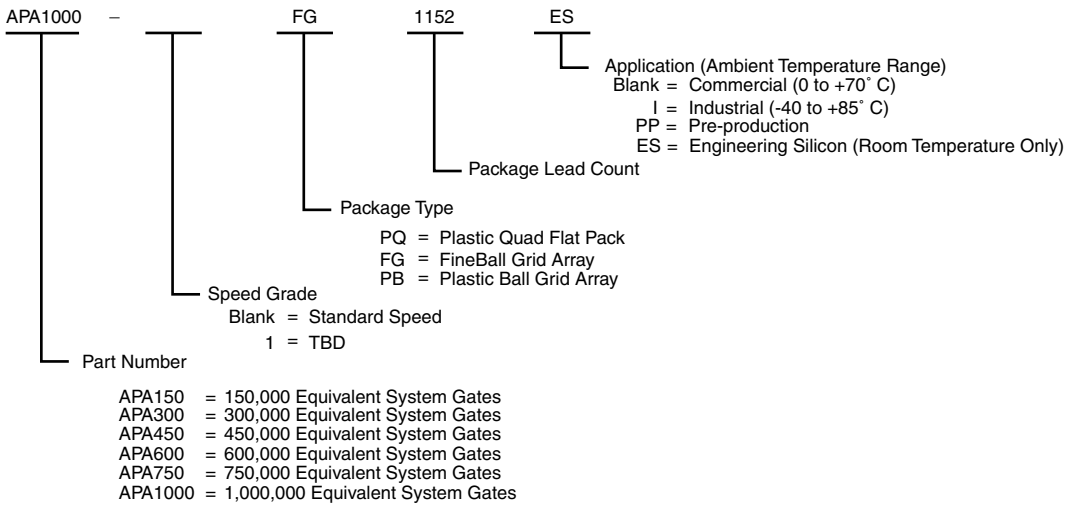
The clock conditioning circuitry is unique. Devices contain two clock conditioning blocks, each with a PLL core, delay lines, phase shifts (0×, 90×, 180×, 270×), and clock multipliers/dividers. In short, this is all the circuitry needed to provide bidirectional access to the PLL, and operation up to 240 MHz. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 4ns (in increments of 0.25ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high speed clock and data inputs.

To support customers' needs for more comprehensive, lower cost board-level testing, Actel's ProASIC^{PLUS} devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more details on the Flash FPGA implementation please refer to the "Boundary Scan" section on page 12.

ProASIC^{PLUS} devices are available in a variety of high-performance plastic packages. Those packages, and the performance features discussed above, are described in more detail in the following sections of this document:

- For more information concerning In-System Programming with ProASIC^{PLUS}, refer to the application note, *Performing Internal In-System Programming Using Actel's ProASIC^{PLUS} Devices*. http://www.actel.com/appnotes/PAplusISPAN.pdf

Ordering Information



Product Plan

	Speed Grade		Application	
	Std	–1	C	I
APA150 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	P	P	P	P
144-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
256-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
APA300 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	P	P	P	P
144-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
256-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
APA450 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	P	P	P	P
144-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
256-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
APA600 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	P	P	P	P
256-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
676-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
APA750 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
456-Pin Fine Ball Grid Array (PBGA)	✔	P	P	P
676-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
896-Pin Plastic Ball Grid Array (FBGA)	P	P	P	P
APA1000 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
896-Pin Plastic Ball Grid Array (FBGA)	P	P	P	P
1152-Pin Plastic Ball Grid Array (FBGA)	P	P	P	P

Applications: *C = Commercial* *I = Industrial*

Availability: P = *Planned* ✔ = *Limited Availability – Contact your Actel Sales representative for the latest availability information.*

Plastic Device Resources

	User I/Os						
Device	**PQFP 208-Pin**	**PBGA 456-Pin**	**FBGA 144-Pin**	**FBGA 256-Pin**	**FBGA 676-Pin**	**FBGA 896-Pin**	**FBGA 1152-Pin**
APA150	158	242	100	186			
APA300	158	290	100	186			
APA450	158	344	100	186			
APA600	158	356		186	454		
APA750	158	356			454	562	
APA1000	158	356				642	712

Package Definitions

PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Ball Grid Array

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core (Figure 1) consists of a Sea-of-Tiles™. Each tile can be configured as a 3-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 2 on page 6 and Figure 3 on page 6). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Table 3 on page 14 lists the 24 basic memory configurations.

Flash Switch

Unlike SRAM FPGAs, ProASIC^PLUS *uses a live on power-up ISP Flash switch as its programming element.*

In the ProASIC^PLUS *Flash switch*, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 2 on page 6).

Logic Tile

The logic tile cell (Figure 3 on page 6) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra fast local and efficient long line routing resources). Any three-input one-output logic function, except a three input XOR, can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus the tiles can flexibly map logic and sequential gates of a design.

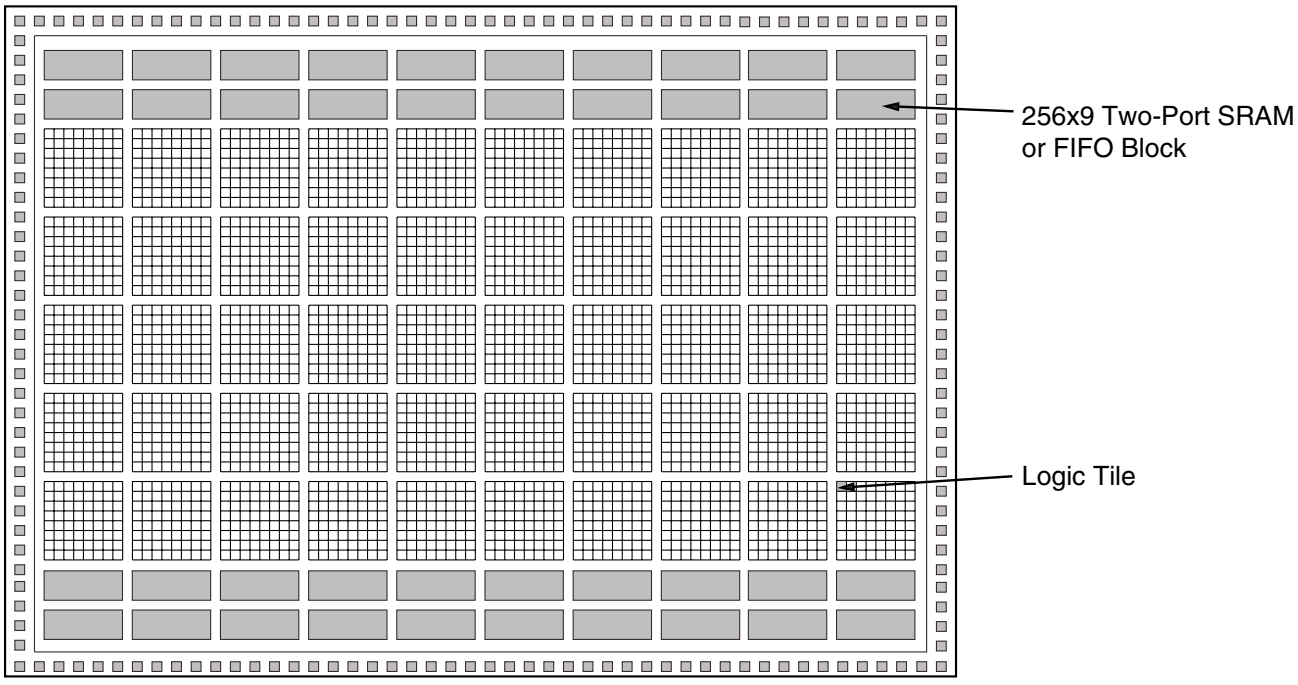


Figure 1 • *The ProASIC^PLUS Device Architecture*

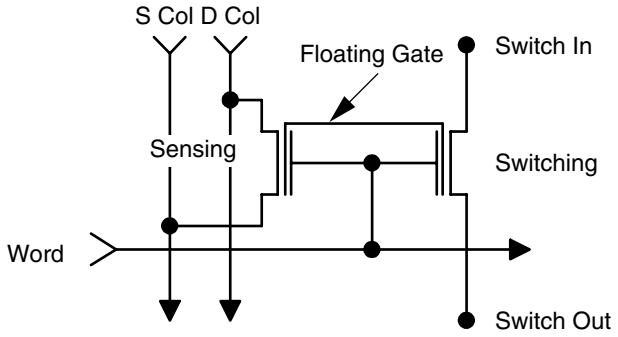


Figure 2 • *Flash Switch*

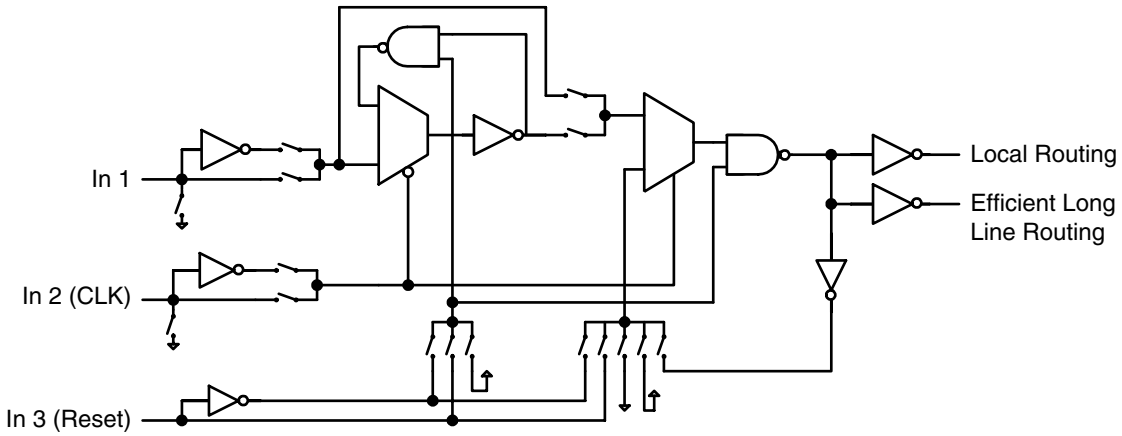


Figure 3 • *Core Logic Tile*

Routing Resources

The routing structure of the ProASIC PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra fast local resources, efficient long line resources, high speed very long line resources, and high performance global networks.

The ultra fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 4 on page 7).

The efficient long line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC PLUS device (Figure 5 on page 7). Each tile can drive signals onto the efficient long line resources, which can, in turn, access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high speed very long line resources which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 6 on page 8).

The high performance global networks are low skew, high fanout nets that are accessible from external pins or from internal logic (Figure 7 on page 9). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all tiles.

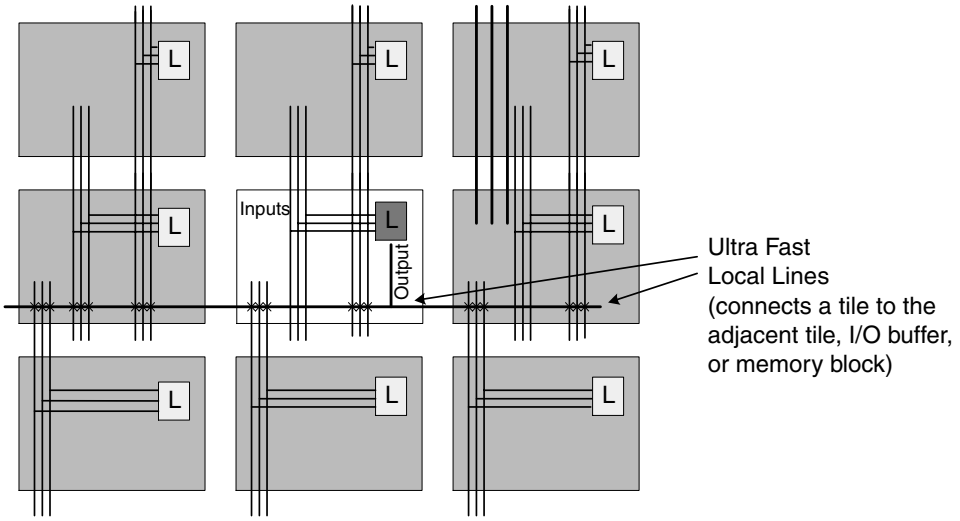


Figure 4 • *Ultra Fast Local Resources*

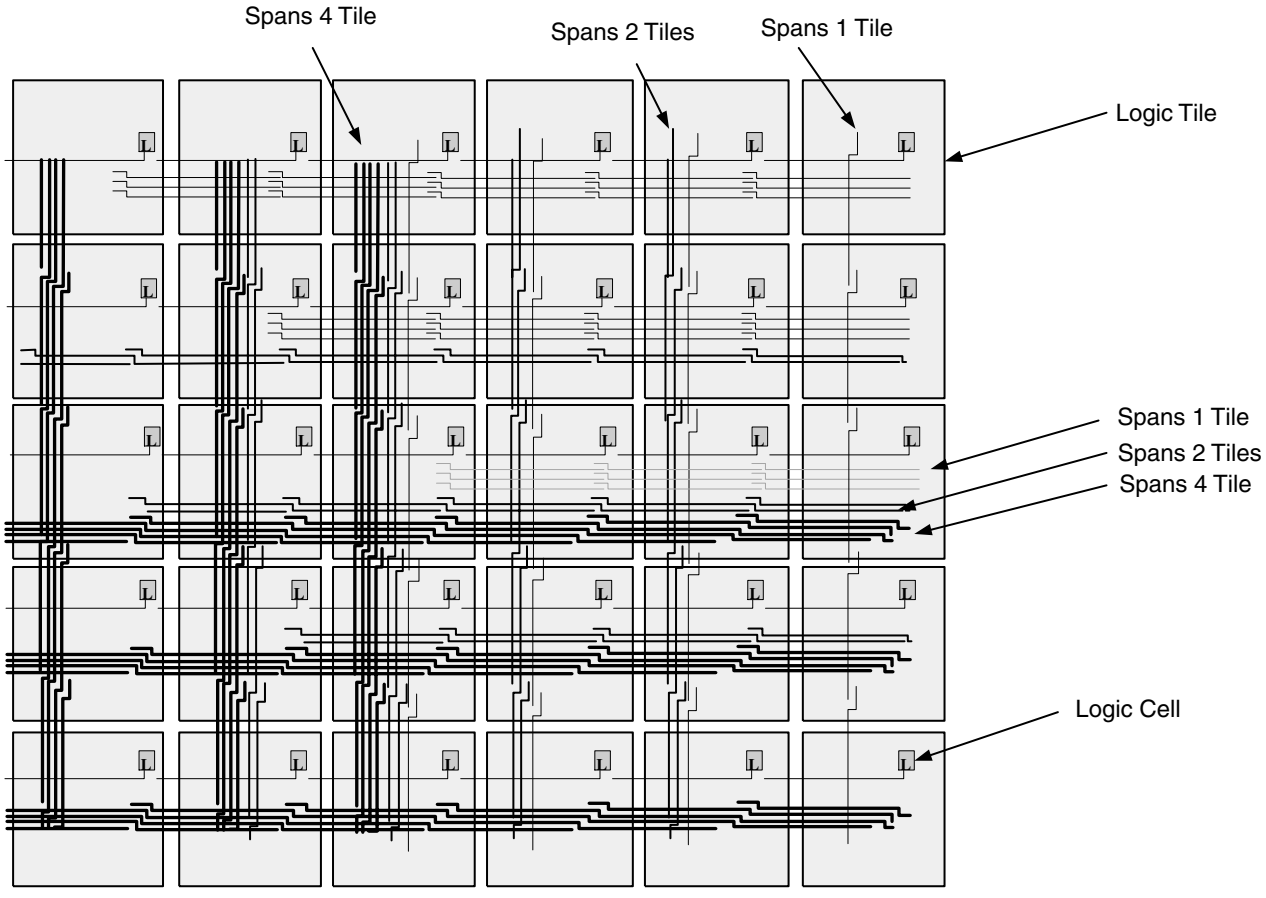


Figure 5 • *Efficient Long Line Resources*

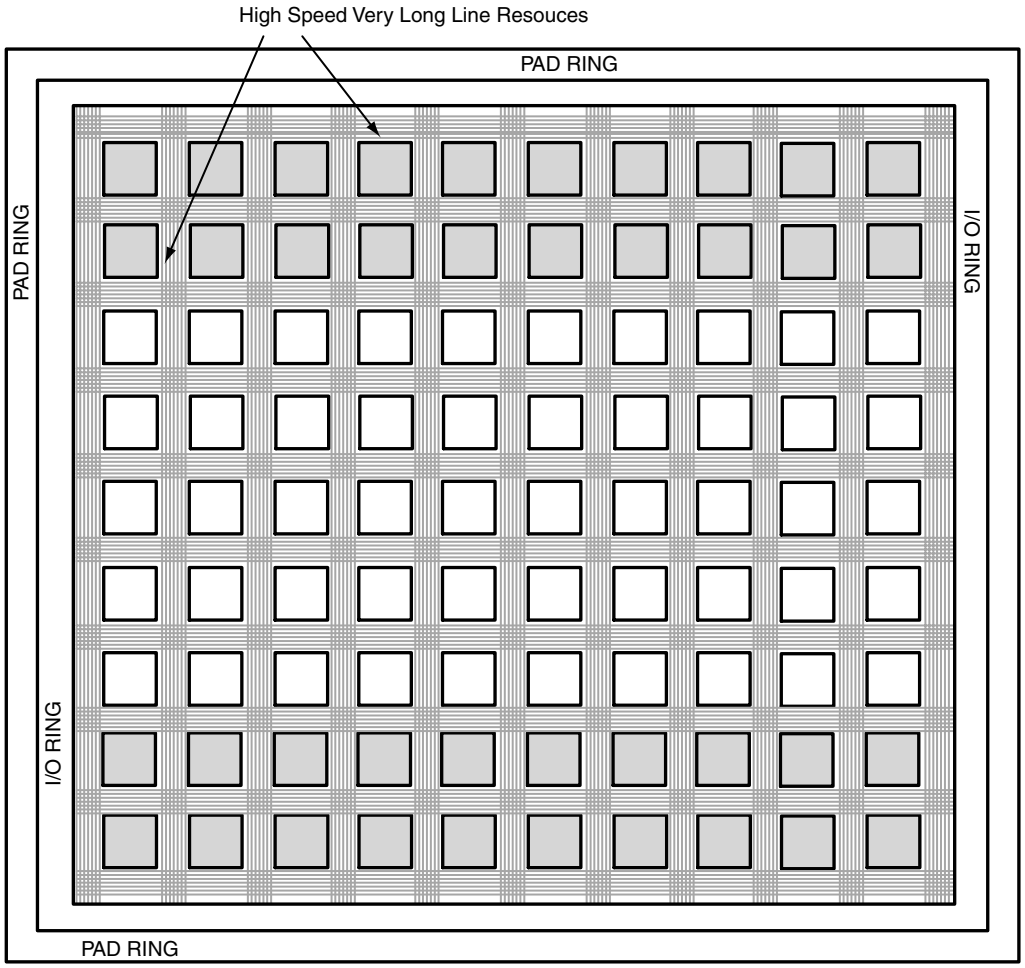


Figure 6 • *High Speed Very Long Line Resources*

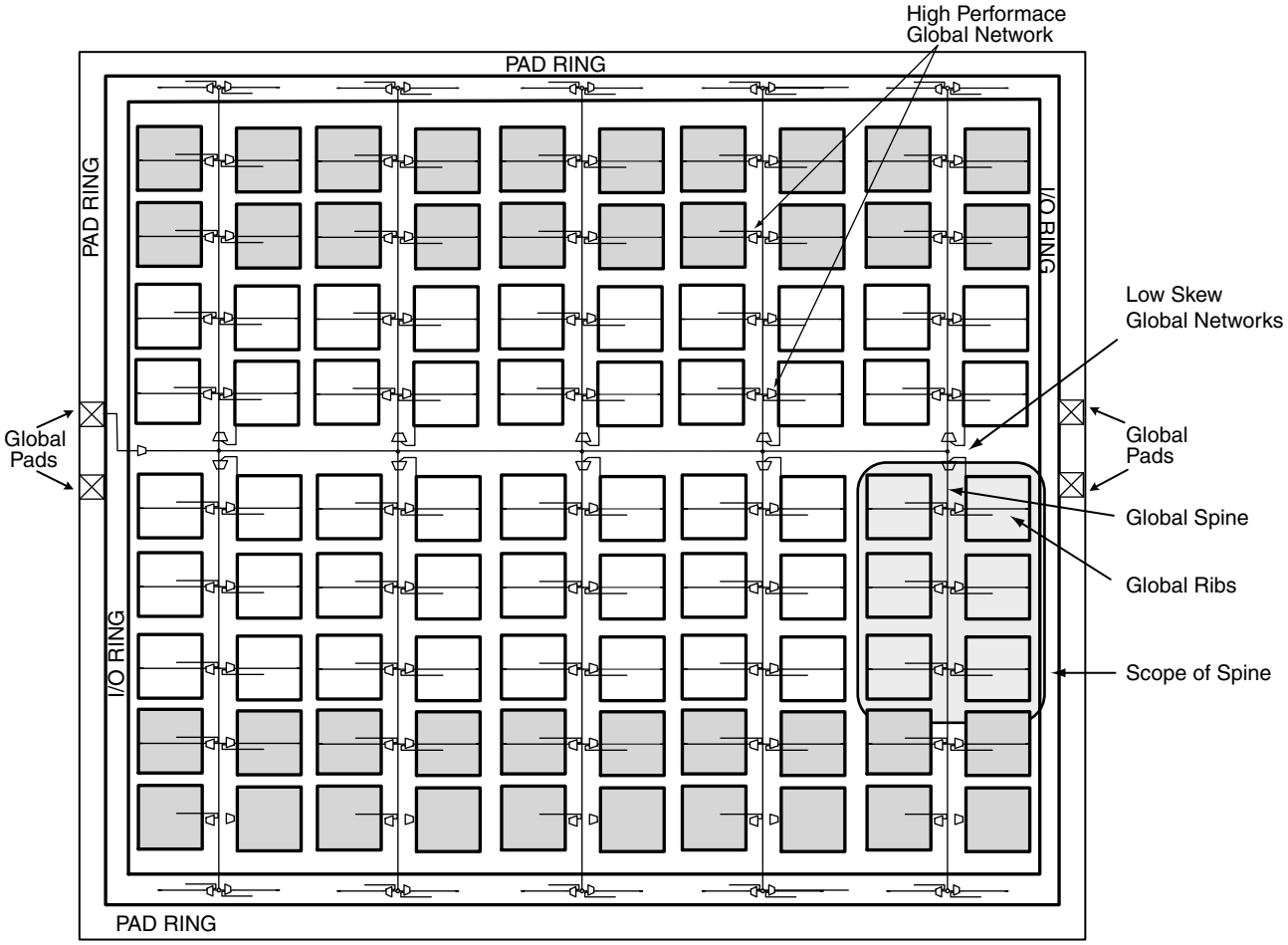
Clock Resources

The ProASIC^PLUS family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks, containing a 240 MHz phase lock loop (PLL) core, delay lines, phase shifter(0°, 90°, 180°, 270°), clock multiplier/dividers and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail later in the data sheet.

Clock Trees

One of the main architectural benefits of ProASIC^PLUS is the set of power and delay friendly global networks. ProASIC^PLUS offers 4 global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 7). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 1 on page 10.

The flexible use of the ProASIC^PLUS clock spine allows the designer to cope with several design requirements. Users implementing clock resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high-fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.



Note: This figure shows routing for only one global path.

Figure 7 • High Performance Global Network

Table 1 • Number of Clock Spines

	APA150	APA300	APA450	APA600	APA750	APA1000
Top Spine Height	24	32	32	48	64	80
Tiles in Each Top Spine	768	1,024	1,024	1,536	2,048	2,560
Bottom Spine Height	24	32	32	48	64	80
Tiles in Each Bottom Spine	768	1,024	1,024	1,536	2,048	2,560
Global Clock Networks (Trees)	4	4	4	4	4	4
Clock Spines/Tree	8	8	12	14	16	22
Total Spines	32	32	48	56	64	88
Total Tiles	6,144	8,192	12,288	21,504	32,768	56,320

Input/Output Blocks

To meet complex system demands, the ProASIC PLUS family offers devices with a large number of user I/O pins, up to 712 on the APA1000. If the I/O pad is powered at 3.3V, each I/O can be selectively configured at the 2.5V and 3.3V threshold levels. Table 2 shows the available supply voltage configurations (the PLL block uses an independent 2.5V supply). Figure 8 illustrates I/O interfaces with global networks. All I/Os include ESD protection circuits. Each I/O has been tested to 2000V to the human body model (per MIL-STD-883, Method 3015).

Six or seven standard I/O pads are grouped with a GND pad and either a V_{DD} or V_{DDP} pad. Two reference bias signals ring the chip. One protects the cascaded output drivers while the other creates a virtual V_{DD} supply for the I/O ring.

Table 2 • ProASIC PLUS Power Supply Voltages

V_{DDP}	2.5V	3.3V
Input Tolerance	2.5V	3.3V, 2.5V
Output Drive	2.5V	3.3V, 2.5V

Notes:

1. *V_{DD} is always 2.5V.*
2. *There is no requirement for power-supply sequencing for ProASIC PLUS devices.*

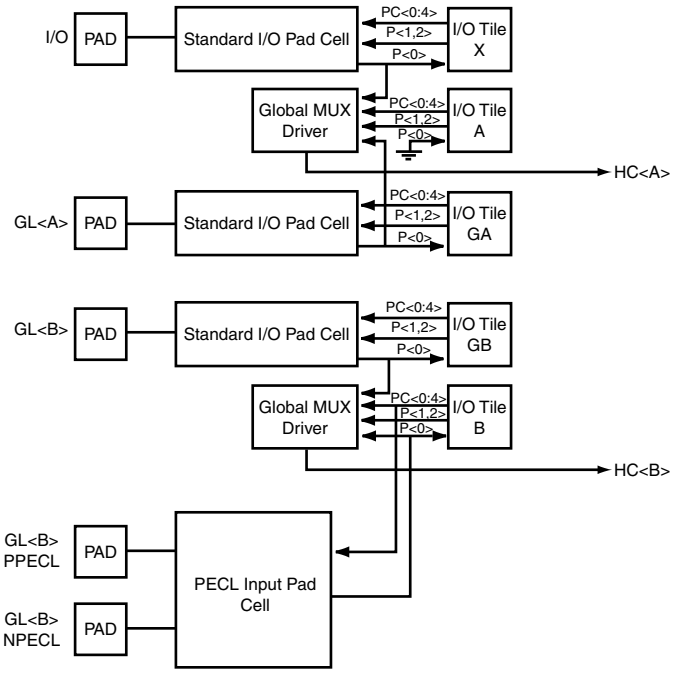


Figure 8 • ProASIC PLUS Global I/O Scheme with Multiplexed Global Pads

I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer (Figure 9). I/O pads configured as inputs have the following features:

- Individually selectable 2.5V or 3.3V threshold levels[1]
- Optional pull-up resistor

I/O pads configured as outputs have the following features:

- Individually selectable 2.5V or 3.3V compliant output signals[1]
- 3.3V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Selectable drive strengths
- Selectable slew rates
- Tristate

I/O pads configured as bidirectional buffers have the following features:

- Individually selectable 2.5V or 3.3V output signals and threshold levels[1]
- 3.3V PCI compliant
- Optional pull-up resistor
- Optionally configurable as Schmitt Trigger input[2]
- Selectable drive strengths
- Selectable slew rates
- Tristate

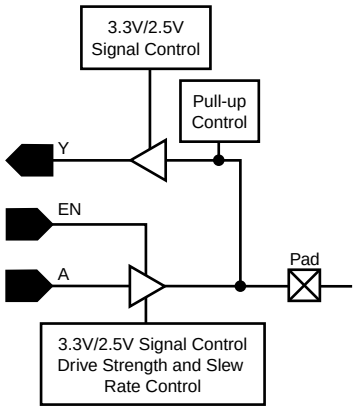


Figure 9 • I/O Block Schematic Representation

1. If pads are configured for 2.5V operation, they are compliant with 2.5V level signals as defined by JEDEC JESD 8-5. If pads are configured for 3.3V operation, they are compliant with the standard as defined by JEDEC JESD 8-A (LVTTL and LVCMOS).

2. The Schmitt Trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has typical hysteresis of about ±0.3V.

LVPECL Input Pads

In addition to standard I/O pads and power pads, ProASIC^PLUS devices have a PECL input pad at each end of each of the global MUX lines, along with AVDD and AGND pins to power the PLL block. The PECL input pad cell is different from the standard I/O cell. It is operated from V_{DD} only. Since it is exclusively an input, it requires no output signal, output enable signal or output configuration bits. As a special high-speed differential input, it also does not require pull ups.

The PECL pad cell (Figure 10) consists of an input buffer (containing a low voltage differential amplifier, whose power is enabled by the PC<0> and CL<1> signals, and a cascaded buffer), and a signal and its compliment (PPECL and NPECL). The PECL pad cell compares voltages on the PPECL pad and the NPECL pad and sends the results to the global MUX over the P<0> wire. This high speed, low skew output essentially controls the clock conditioning circuit.

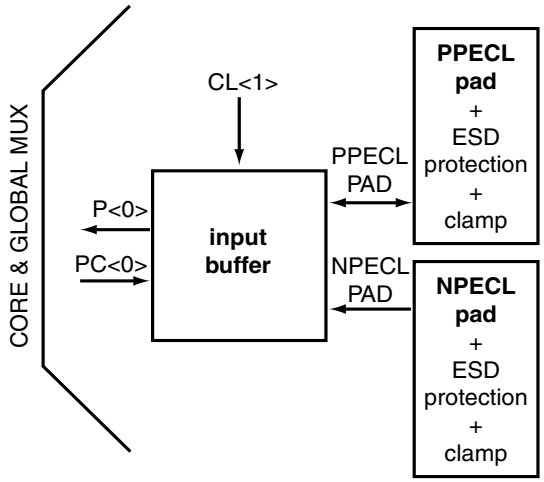


Figure 10 • High Speed PECL Pad Cell Block Diagram

Boundary Scan

ProASIC^PLUS devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic ProASIC^PLUS boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 11). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS), the optional IDCODE instructions and private instructions used for device programming and factory testing.

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 12 on page 13. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

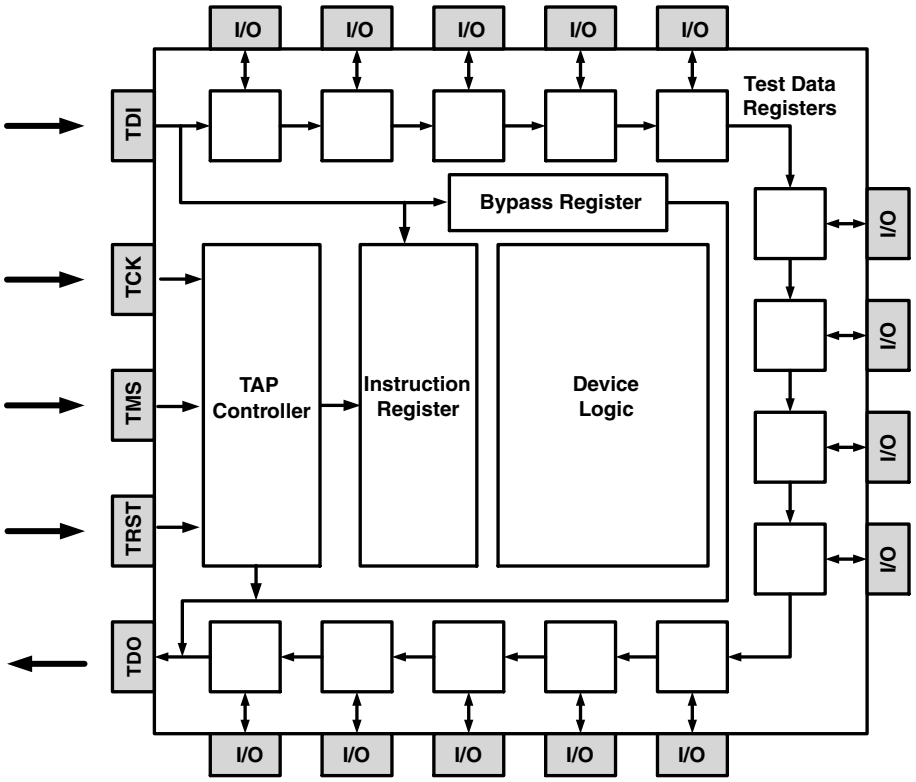


Figure 11 • ProASIC^PLUS JTAG Boundary Scan Test Logic Circuit

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC*PLUS* devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pins. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary scan register chain which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

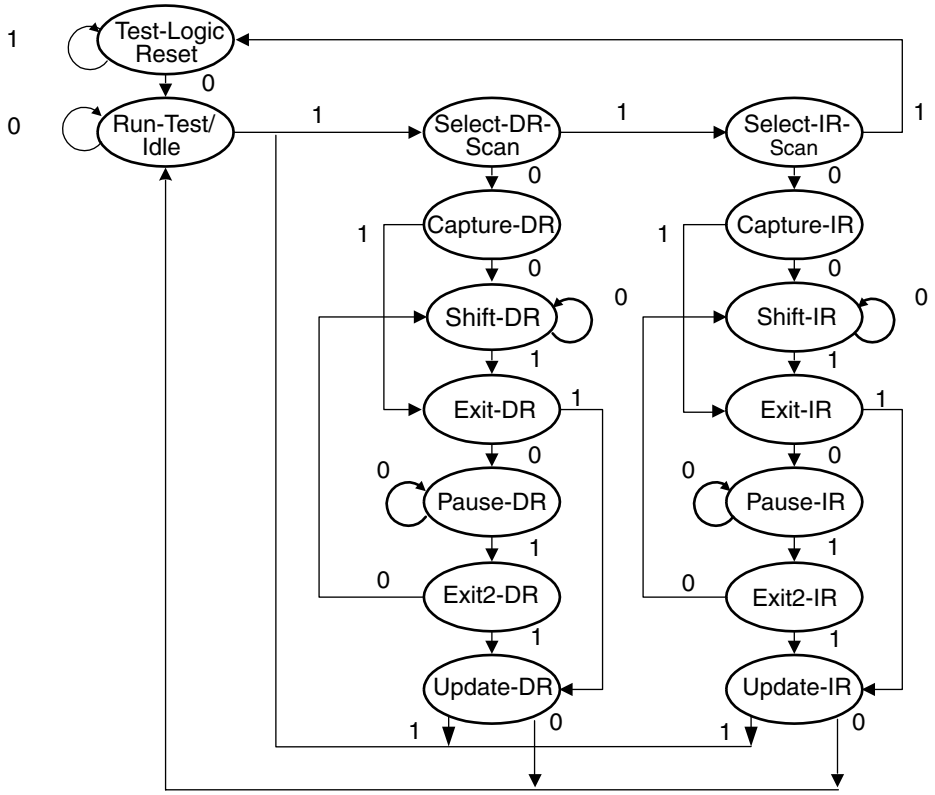


Figure 12 • *TAP Controller State Diagram*

User Security

The ProASIC^PLUS devices have read-protect bits that, once programmed, block the entire programmed contents from being read externally. If locked, the user can only reprogram the device using the security key. This protects it from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (which are actually very small capacitors), rather than in the wiring, physical deconstruction cannot be used to compromise data. This approach is further hampered by the placement of the memory cells, beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Embedded Memory Floorplan

The embedded memory is located across the top of the device (see Figure 1 on page 5) in 256x9 blocks. Depending upon the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory or combined (using dedicated memory routing resources) to form larger, more complex memories. A single memory configuration cannot include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

The embedded memory in the ProASIC^PLUS family provides great configuration flexibility. Other programmable vendors typically use single port memories that can only be transformed into two-port memories by sacrificing half the memory. Each ProASIC^PLUS block is designed and optimized as a two-port memory (1 read, 1 write). This provides 198k bits of total memory for two-port and single port usage in the APA1000 device.

Each memory can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 3). Additional characteristics include programmable flags as well as parity checking and generation. Figure 13 on page 15 and Figure 14 on page 16 show the block diagrams of the basic SRAM and FIFO blocks. These memories are designed to operate at up to 150 MHz when operated individually. Each block contains a 256 word, 9-bit wide (1 read, 1 write) memory. The memory blocks may be combined in parallel to form wider memories or stacked to form deeper memories (Figure 15 on page 16). This provides optimal bit widths of 9 (1 block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1024. Refer to the Actel's *Macro Library Guide* for more information.

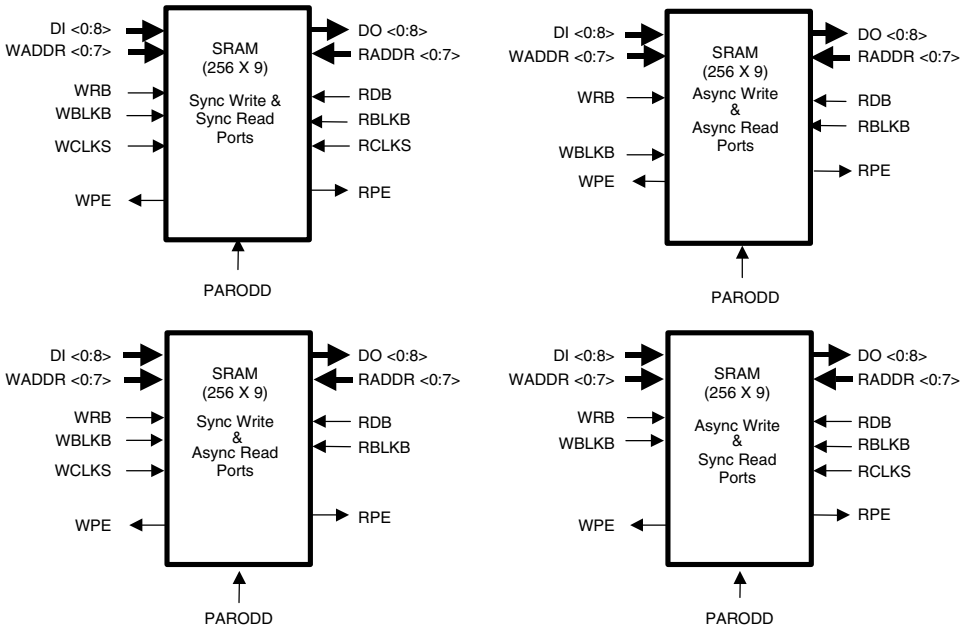
Figure 16 on page 17 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three memories of various widths and depths. Figure 17 on page 17 shows how memory can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port memories. The Actel ACTgen software facilitates building wider and deeper memories for optimal memory usage.

Table 3 • *Basic Memory Configurations*

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256x9AST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256x9ASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256x9AA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256x9AST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP

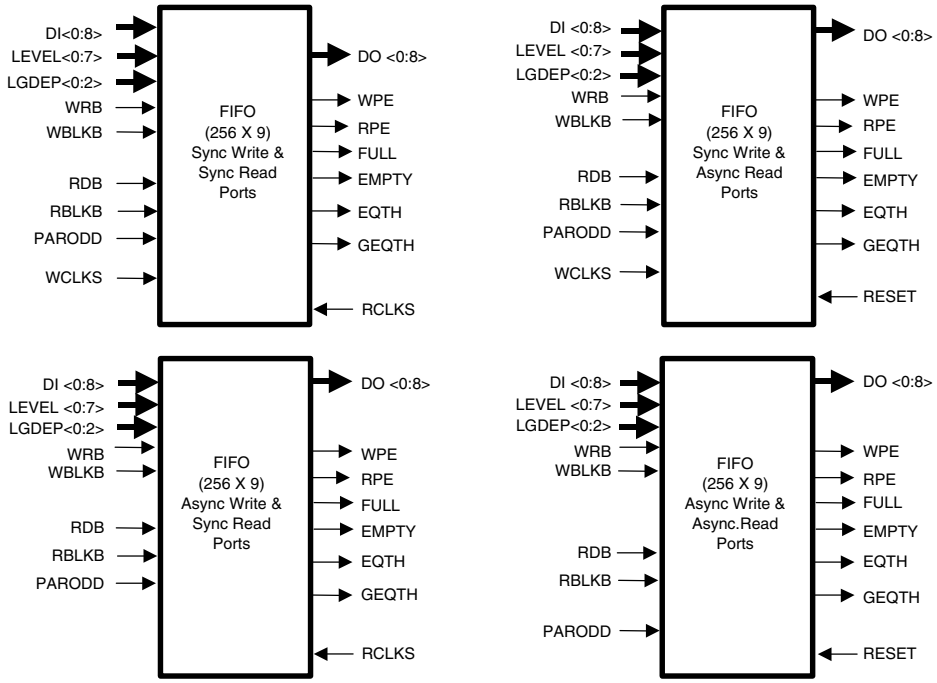
Table 3 • Basic Memory Configurations (Continued)

Type	Write Access	Read Access	Parity	Library Cell Name
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256x9SAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP



Note: *For memory block interface signal definitions, see Table 4 on page 35*

Figure 13 • Example SRAM Block Diagrams



Note: *For memory block FIFO signal definitions, see Table 5 on page 46.*

Figure 14 • Basic FIFO Block Diagrams

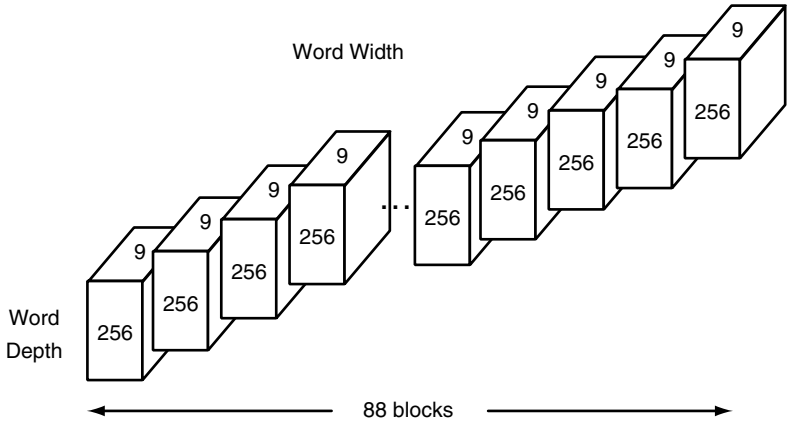


Figure 15 • APA1000 Memory Block Architecture

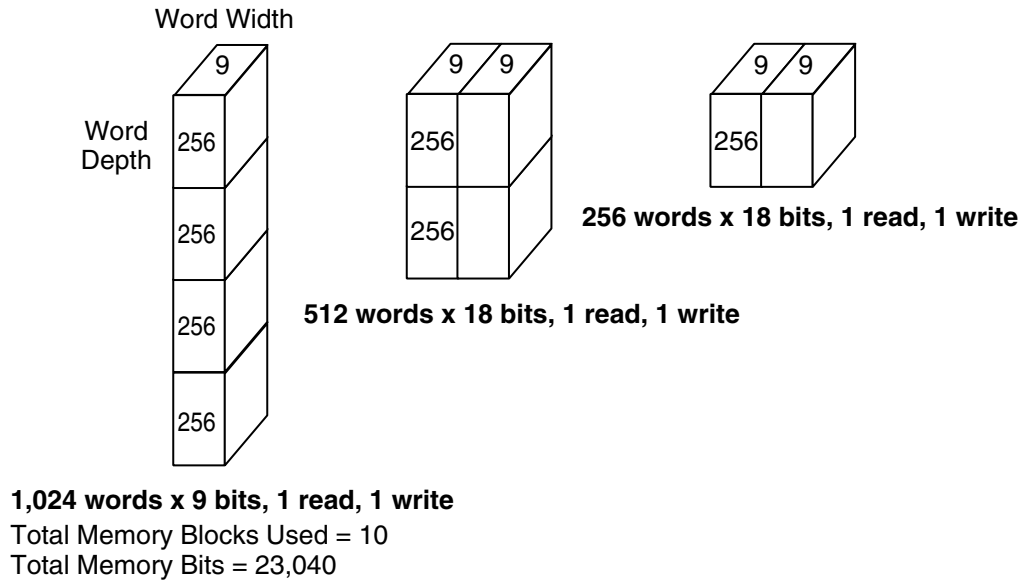


Figure 16 • *Example Showing Memories with Different Widths and Depths*

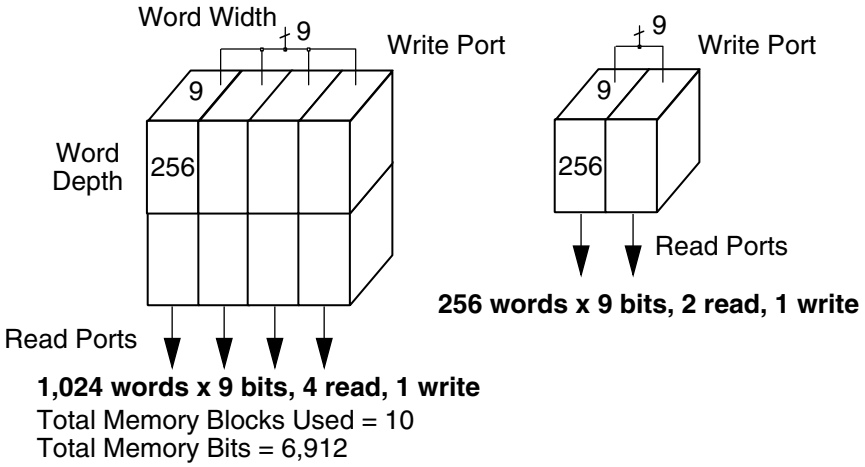


Figure 17 • *Multiport Memory Usage*

Design Environment

ProASIC^PLUS devices are supported by Actel's Designer Series, as well as third party CAE tools. Unlike some FPGA vendors, no special HDL design techniques are needed when using the standard VHDL or Verilog HDL descriptions. As a result, designers may utilize technology independent of HDL code for ProASIC^PLUS devices. This feature and the ASIC-like design flow ensure a seamless transition to an ASIC implementation, if desired (Figure 18 on page 18).

ACTgen, included in Actel's Designer Series, can be used to automatically generate memories based on user inputs. The design engineer can select the depth and width, usage of parity generation or check, and synchronous or asynchronous functionality of the ports. For a synchronous read port, the user can choose whether the output is pipelined or transparent. Designer allows any bit width up to 252. However, when an intermediate bit width, such as 16 bits, is chosen, the remaining two bits are not accessible for other memories. Actel's Designer also enables optimal memory stacking in 256 word increments. However, any word depth may be combined for up to 22,528 words. ACTgen also allows the user to generate distributed memory.

Place and route is also performed by Actel's Designer software. Available for UNIX workstations and PC platforms, Designer accepts standard netlists in Verilog, VHDL, and EDIF formats, performs place and route of the design into the selected device, and provides postlayout delay information for back-annotation simulation and static timing analysis.

ACTgen provides all the software needed for configuration of the PLL clock conditioning circuit. While the PLL has no placement mobility, ACTgen allows users to use placement and routing floorplan constraints hierarchically, in order to more easily and efficiently explore floorplan alternatives. This allows the power of the PLL circuitry to be utilized with minimal top level timing loop iterations.

Actel's Designer can also generate the BSDL (boundary-scan description language) files required for documenting the IEEE 1149.1 components which can be used by automatic test equipment software.

Actel's Designer also contains the necessary information for the placing, routing, and configuration of the clock conditioning circuit.

Once the design is finalized, the programming bitstream is downloaded into the device programmer for programming the ProASIC^{PLUS} part. ProASIC^{PLUS} devices can be programmed with the Silicon Sculptor II and Flash Pro programmers. Additionally, in-system programming is available. For details on ProASIC^{PLUS} programming, refer to the application note, *Performing Internal In-System Programming Using Actel's ProASIC^{PLUS} Devices*.

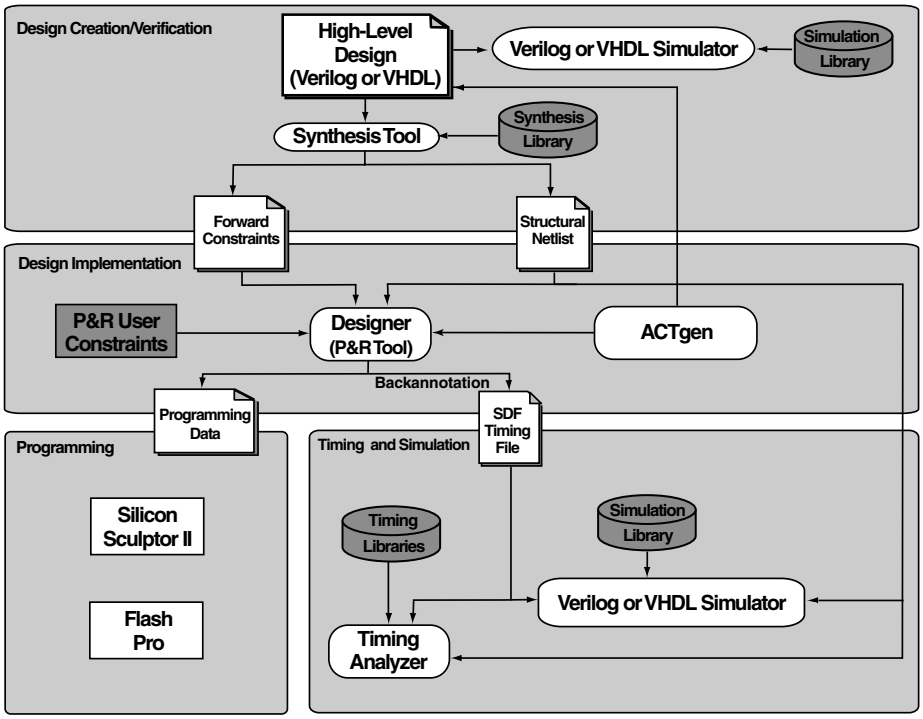


Figure 18 • *Design Flow*

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package, to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

Θ_{ja} is a function of the rate (in linear feet per minute - lfpm) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used.

Package Type	Pin Count	Θ_{jc}	Θ_{ja} Still Air	Θ_{ja} 300 ft./min	Units
Plastic Quad Flat Pack (PQFP)	208	8	30	23	°C/W
PQFP with Heatspreader	208	3.8	20	17	°C/W
Fine Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Ball Grid Array (FBGA)	256	3.0	30	25	°C/W
Plastic Ball Grid Array (PBGA)	456	3	18	14.5	°C/W
Fine Ball Grid Array (FBGA)	676	3.2	15	11.5	°C/W
Fine Ball Grid Array (FBGA)	896	2.0	10.9	7.9	°C/W
Fine Ball Grid Array (FBGA)	1152	2.0	11.2	7.0	°C/W

Calculating Power Dissipation

ProASIC PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

$$P_{total} = P_{dc} + P_{ac}$$

where:

- P_{dc} = 10 mW
- P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{ios} + P_{memory}$

P_{clock}, the clock component of power dissipation, is given by

$$P_{clock} = (P1 + P2 * s) * Fs$$

where:

- P1 = 2500 uW/MHz is the basic power consumption of the clock tree normalized per MHz of the clock.
- P2 = 1.0 uW/MHz is the extra power consumption of the clock tree per storage tile – also normalized per MHz of the clock
- s = the number of storage tiles clocked by this clock
- Fs = the clock frequency

$P_{storage}$, the storage-tile component of AC power dissipation, is given by

$$P_{storage} = P5 * ms * Fs$$

where:

- P5 = 1.0 uW/MHz is the average power consumption of a storage-tile normalized per MHz of its output frequency
- ms = the number of storage tiles switching during each Fs cycle
- Fs = the clock frequency

P_{logic}, the logic-tile component of AC power dissipation, is given by

$$P_{logic} = P3 * mc * Fs$$

where:

- P3 = 3.0 uW/MHz, is the average power consumption of a logic-tile normalized per MHz of its output frequency
- mc = the number of logic tiles switching during each Fs cycle
- Fs = the clock frequency

P_{ios}, the I/O component of AC power dissipation, is given by

$$P_{ios} = (P4 + C_{load} * V_{ddp}\text{^}2) * p * Fp$$

where:

- P4 = 60.0 uW/MHz is the average power consumption of an output pad normalized per MHz of its output frequency (internal power-load is not included)
- C_{load} = the output load
- p = the number of outputs
- Fp = the average output frequency

Finally, P_{memory}, the memory component of AC power consumption, is given by

$$P_{memory} = P6 * N_{mem} * F_{mem}$$

where:

- P6 = 100.0 uW/MHz is the average power consumption of a memory block normalized per MHz of the clock
- N_{mem} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)
- F_{mem} = the clock frequency of the memory

The following is an APA750 example using a shift register design with 13,440 storage tiles and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

- Fs = 10 MHz
- s = 13,440

=> Pclock = (P1 + P2 * s) * Fs = 159.4 mW

$P_{storage}$

- ms = 13,440 (in a shift register 100% of storage-tiles are toggling at each clock cycle and Fs = 10 MHz)
- mc = 0 (no logic tile in this shift-register)

=> Pstorage = P5 * ms * Fs = 134.4 mW

P_{logic}

- C_{load} = 40 pF
- V_{ddp} = 3.3 V
- p = 24

=> P_{logic} = 0 mW

P_{ios}

- Fp = 5 MHz

=> P_{ios} = (P4 + Cload * V_{ddp}^2) * p * Fp = 54.1 mW

P_{memory}

N_{mem} = 0 (no RAM/FIFO in this shift-register)

=> P_{memory} = 0 mW

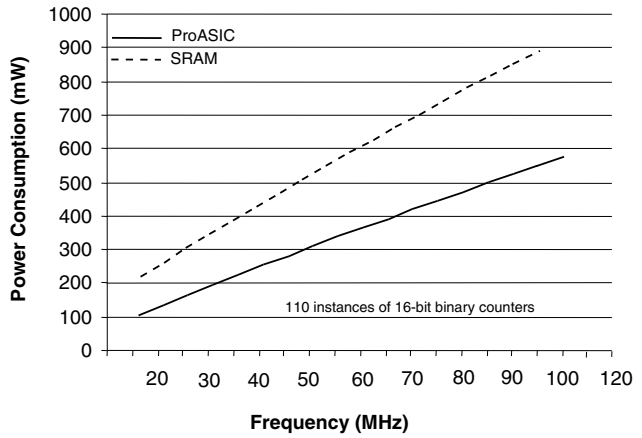
P_{ac}

=> 347.9 mW

P_{total}

P_{dc} + P_{ac} = 357.9mW

Power Consumption of an APA Device



Operating Conditions

Absolute Maximum Ratings

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–0.5	V_{DDP} + 0.5	V
DC Input Clamp Current	V_{IN} < 0 or V_{IN}> V_{DDP}	–10	+10	mA
PECL Input Voltage		0	2.5	V

Programming and Storage Temperature Limits

Product Grade	Programming Cycles	Program Retention	Storage Temperature	
			Min.	Max.
Commercial	100	20 years	–55°C	110°C
Industrial	100	20 years	–55°C	110°C

Supply Voltages

Mode	V_{DD}	V_{DDP}	V_{PP}	V_{PN}
Single Voltage	2.5V	2.5V	$0 \le V_{PP} \le 16.5V$	$–13.8V \le V_{PN} \le 0V$
Mixed Voltage	2.5V	3.3V	$0 \le V_{PP} \le 16.5V$	$–13.8V \le V_{PN} \le 0V$

Recommended Operating Conditions

Parameter	Symbol	Limits
Commercial		
DC Supply Voltage (2.5V I/Os)	V_{DD} & V_{DDP}	2.3V to 2.7V
DC Supply Voltage (Mixed 2.5V, 3.3V I/Os)	V_{DDP} V_{DD}	3.0V to 3.6V 2.3V to 2.7V
Operating Ambient Temperature Range	T_A	0°C to 70°C
Maximum Operating Junction Temperature	T_J	110°C
Maximum Clock Frequency	f_{CLOCK}	240 MHz
Maximum RAM Frequency	f_{RAM}	150 MHz
Industrial		
DC Supply Voltage (2.5V I/Os)	V_{DD} & V_{DDP}	2.3V to 2.7V
DC Supply Voltage (2.5V, 3.3V I/Os)	V_{DDP} V_{DD}	3.0V to 3.6V 2.3V to 2.7V
Operating Ambient Temperature Range	T_A	–40°C to 85°C
Maximum Operating Junction Temperature	T_J	110°C
Maximum Clock Frequency	f_{CLOCK}	240 MHz
Maximum RAM Frequency	f_{RAM}	150 MHz

DC Electrical Specifications (V_{DDP} = 2.5V +/-0.2V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OH} = –6 mA I_{OH} = –12 mA I_{OH} = –24 mA I_{OH} = –4 mA I_{OH} = –6 mA I_{OH} = –10 mA	 2.1 2.0 1.7 2.1 2.0 1.7			V
V_{OL}	Output Low Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OL} = 8 mA I_{OL} = 15 mA I_{OL} = 24 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 15 mA			 0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage		1.7		V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq 1.25$	10		30	kΩ
I_{IN}	Input Current Input Current	with pull up (V_{IN} = V_{SS}) without pull up (V_{IN} = V_{SS} or V_{DD})	–250 –10		– 80 10	µA µA
I_{DDQ}	Quiescent Supply Current (standby)	V_{IN} = V_{SS}[2] or V_{DD}		5.0	10	mA
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DD}	–10		10	µA
I_{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{SS} V_{IN} = V_{SS}	 –120 –100			mA
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{DDP} V_{IN} = V_{DDP}			 100 30	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. All process conditions. Junction Temperature: –40 to +110°C.

2. No pull-up resistor.

DC Electrical Specifications (V_{DDP} = 3.3V +/-0.3V and V_{DD} 2.5+/-0.2V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3V I/O, High Drive (OB33P)	I_{OH} = –15 mA I_{OH} = –30 mA	0.9∗V_{DDP} 2.4			V
	3.3V I/O, Low Drive (OB33L)	I_{OH} = –7 mA I_{OH} = –14 mA	0.9∗V_{DDP} 2.4			
	Output High Voltage 2.5V I/O, High Drive (OB25H)	I_{OH} = –0.1 mA I_{OH} = –0.5 mA I_{OH} = –4 mA	2.1 2.0 1.7			V
	2.5V I/O, Low Drive (OB25L)	I_{OH} = –0.1 mA I_{OH} = –0.5 mA I_{OH} = –2.5 mA	2.1 2.0 1.7			
V_{OL}	Output Low Voltage 3.3V I/O, High Drive (OB33P)	I_{OL} = 15 mA I_{OL} = 20 mA			0.1V_{DDP} 0.4	V
	3.3V I/O, Low Drive (OB33L)	I_{OL} = 7 mA I_{OL} = 10 mA			0.1V_{DDP} 0.4	
	Output Low Voltage 2.5V I/O, High Drive (OB25H)	I_{OL} = 7 mA I_{OL} = 14 mA I_{OL} = 28 mA			0.2 0.4 0.7	V
	2.5V I/O, Low Drive (OB25L)	I_{OL} = 5 mA I_{OL} = 10 mA I_{OL} = 15 mA			0.2 0.4 0.7	
V_{IH}	Input High Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		2 1.7		V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		0.3 0.3		0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB33U)	$V_{IN} \geq$ 1.5	15k		25k	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25U)	$V_{IN} \geq$ 1.5	10k		20k	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = V_{SS}) without pull up (V_{IN} = V_{SS} or V_{DD})	–300 –-10		–80 10	µA µA
I_{DDQ}	Quiescent Supply Current (standby)	V_{IN} = V_{SS}[2] or V_{DD}		5.0	10	mA
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DD}	–-10		10	µA
I_{OSH}	Output Short Circuit Current High 3.3V High Drive (OB33P) 3.3V Low Drive (OB33L)	V_{IN} = V_{SS} V_{IN} = V_{SS}			200 100	mA
	2.5V High Drive (OB25H) 2.5V Low Drive (OB25L)	V_{IN} = V_{SS} V_{IN} = V_{SS}			20 10	

Notes:

1. *All process conditions. Junction Temperature: –40 to +110°C.*
2. *No pull-up resistor.*

DC Electrical Specifications (V_{DDP} = 3.3V +/-0.3V and V_{DD} 2.5+/-0.2V) (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{OSL}	Output Short Circuit Current Low 3.3V High Drive 3.3V Low Drive 2.5V High Drive 2.5V Low Drive	 $V_{IN} = V_{DD}$ $V_{IN} = V_{DD}$ $V_{IN} = V_{DD}$ $V_{IN} = V_{DD}$			 2 00 100 2 00 100	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Junction Temperature: –40 to +110°C.*
2. *No pull-up resistor.*

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{DD}	Supply Voltage for Core		2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{DPP}$	V_{DPP} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$	–10	+10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{DPP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{DPP}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

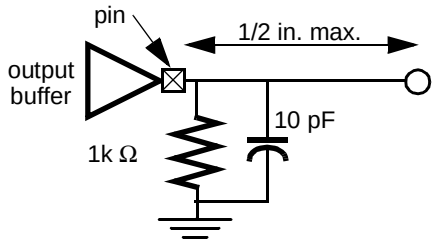
Notes:

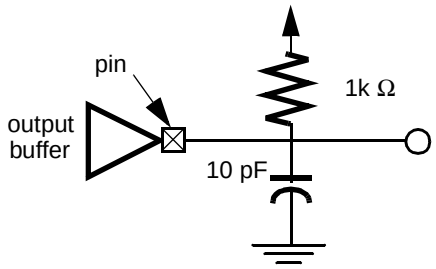
1. *This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (3.3V PCI Revision 2.2 Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ *	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ *	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ *			
	(Test Point)	VOUT = 0.7VCC *		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ *	$16V_{DDP}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ 1	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ *		See page 21, equation B of PCI rev. 2.2 spec	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ *		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load *	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load *	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*





Timing Control and Characteristics

Clock Conditioning Circuit

ProASIC^{PLUS} devices provide designers with very flexible clocking capabilities. Each side of the chip contains a clock conditioning circuit based upon a 240 MHz phase-locked loop (PLL) block (Figure 19 on page 28). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional PECL input pads (described below). The global lines may be driven by either the PECL global input pad or the outputs from the PLL block or both. Each can be driven by a different output from the PLL.

The 2 signals available to drive the global networks are as follows:

Global A:

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT})
  - Delayed or advanced
  - 0°, 90°, 180°, and 270° phase shift (with optional time advance)
- Divided version of either of the above
- Delayed version of either of the above (0.25ns, 0.50ns, or 4.00ns delay).[3]

Global B:

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Delayed version of either of the above (0.25ns, 0.50ns, or 4.00ns delay).[3]

Each PLL block contains four programmable dividers as shown in Figure 20 on page 28. The first (**n**) provides all integer divisors from 1 to 16. The second and third (**u** and **v**) permit the signal applied to the global network to be further divided by factors of 2, 3 or 4. The fourth divider (**m**, located in the direct feedback path) is controlled by 6 bits, allowing the incoming clock signal to be multiplied by integer factors from 1 to 64. The implementations m/(n*u) and m/(n*v) enable the user to define a wide range of multipliers and divisors factors.

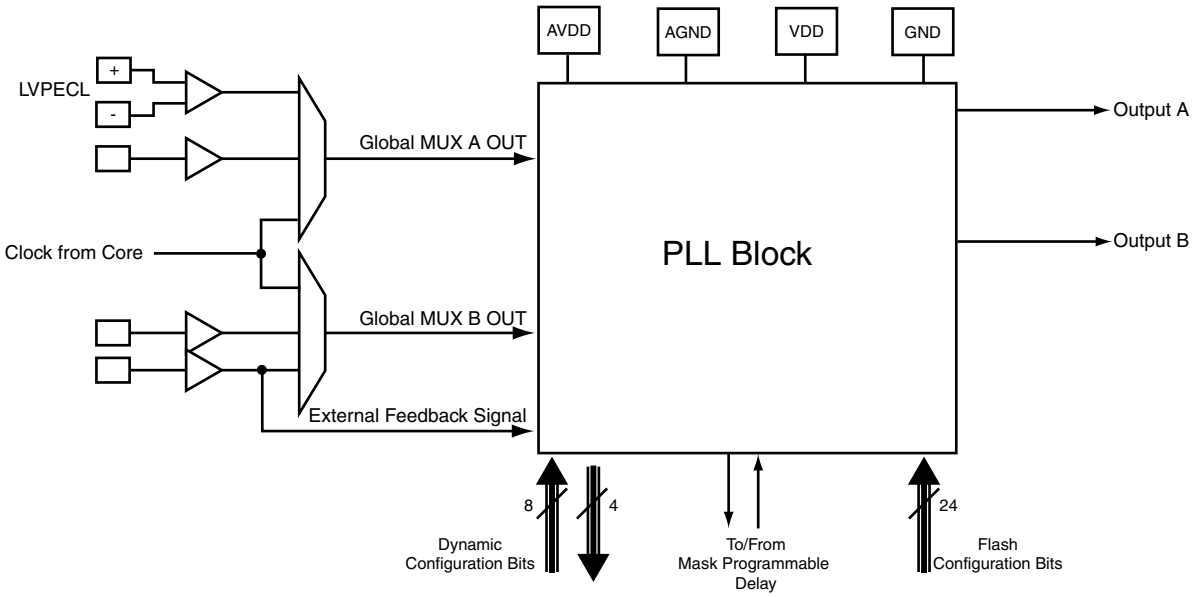
The clock conditioning circuit can advance or delay the clock up to 4ns (in increments of 0.25ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0°, 90°, 180°, and 270°. A "lock" signal is provided to indicate that the PLL has locked to the incoming signal, and a "standby" signal switches the PLL block off when it is not locked to a signal. That allows pre-selected signals to be passed directly through, at least to the corresponding rib drivers.

Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output mode can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.

The PLL can be configured internally during design (via Flash-configuration bits set in the programming bitstream) or externally during operation. This is done through a simple, dynamically accessible asynchronous interface – a dedicated register file, which allows user signals to initiate parameter changes, such as PLL divide/multiply ratios.

For information on the clock conditioning circuit, refer to the, U*sing ProASIC^{PLUS} Clock Conditioning Circuits* application note.

3. This mode is available through the delay feature of the Global MUX driver.



Dynamic Configuration Bit Inputs
Stand-by mode of Core
Data In
Shift Clock
Shift Enable
Update
NVM/Register Mode
(Other three bits used for flash configuration)

Dynamic Configuration Bit Outputs
Lock Detect
Data Out
GND (Spare 1)
GND (Spare 2)

Figure 19 • *PLL Block – Top-Level View*

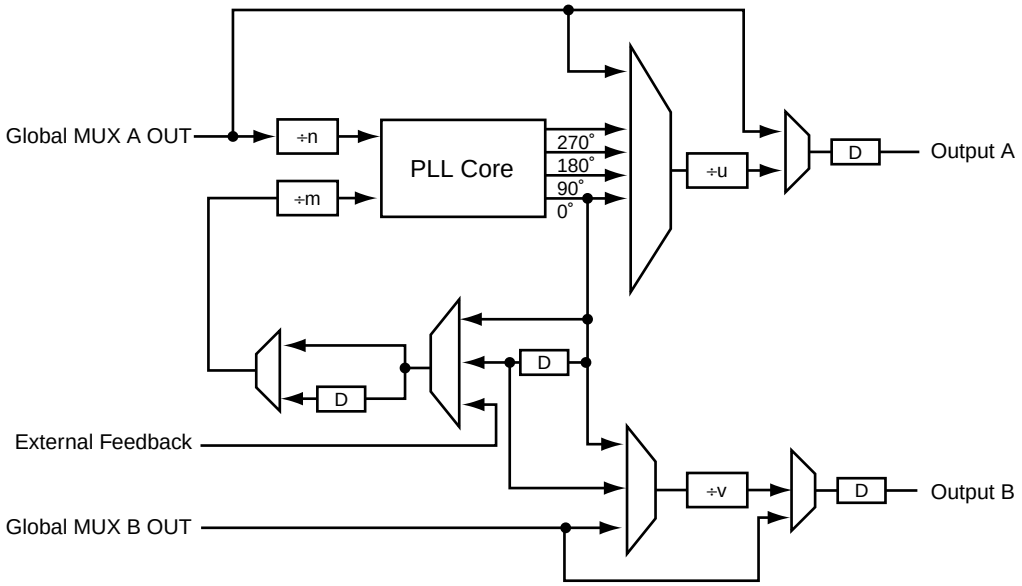


Figure 20 • *PLL Block – Detailed Block Diagram*

Logic Tile Timing Characteristics

Timing characteristics for ProASIC^{PLUS} devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ProASIC^{PLUS} family members. Internal routing delays are device dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90% of the nets in a design are typical. Refer to the Actel *Designer User's Guide* for details on using constraints.

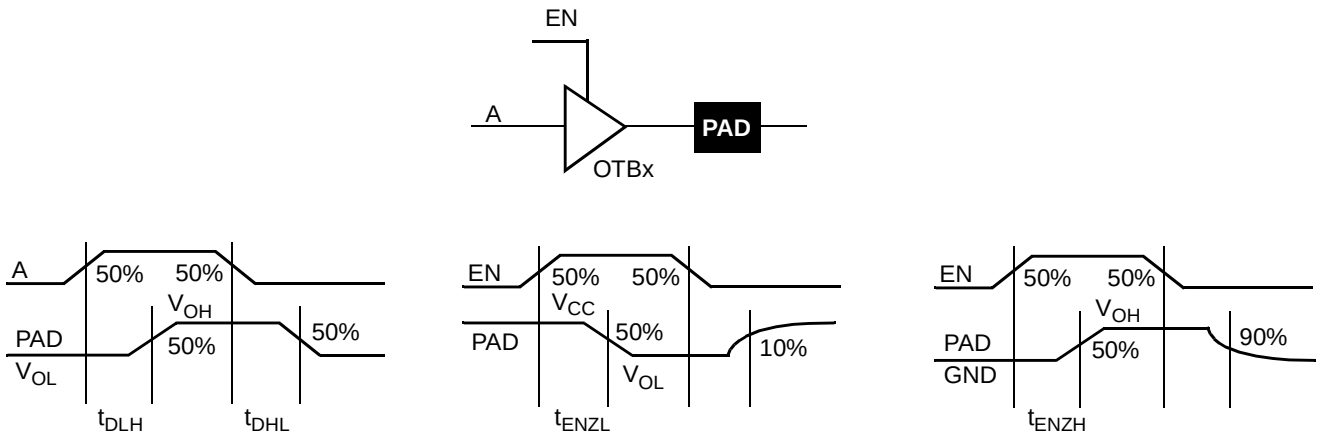
High Speed Very Long Lines

Some nets in the design are very long lines, which are special routing resources that span multiple rows, columns or modules. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require very long lines. Very long lines contribute from 4ns to 8.4ns routing delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

Since ProASIC^{PLUS} devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications).

Tristate Buffer Delays



Tristate Buffer Delays

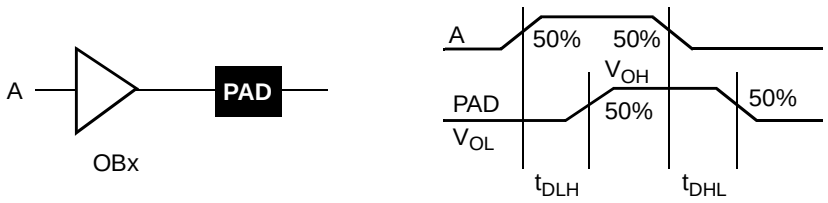
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 70°C)

Macro Type	Description	Max t_{DLH}	Max t_{DHL}	Max t_{ENZH}	Max t_{ENZL}	Units
OTB33PH	3.3V, PCI Output Current, High Slew Rate	2.4	2.2	4.4	3.7	ns
OTB33PN	3.3V, PCI Output Current, Nominal Slew Rate	2.9	2.7	5.0	5.5	ns
OTB33PL	3.3V, PCI Output Current, Low Slew Rate	3.5	3.4	5.5	6.9	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	3.4	3.8	6.2	6.1	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	4.3	4.5	7.0	9.3	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	4.9	6.3	7.8	12.3	ns
OTB25HH	2.5V, High Output Current, High Slew Rate	2.7	2.2	7.2	3.5	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate	3.5	3.2	7.5	5.1	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate	4.2	3.6	8.5	6.4	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate	3.9	4.9	10.8	5.4	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate	5.7	4.6	11.5	8.4	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate	7.1	6.0	12.4	11.1	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	6.0	1.9	5.3	4.6	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	5.9	2.8	6.2	7.7	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	5.9	4.3	7.1	9.7	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	9.2	2.7	7.7	8.1	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	9.2	3.8	8.9	12.8	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	9.2	5.4	10.2	17.4	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*
3. *t_{ENZH} = Enable-to-Pad, Z to HIGH*
4. *t_{ENZL} = Enable-to-Pad, Z to LOW*

Output Buffer Delays



Output Buffer Delays

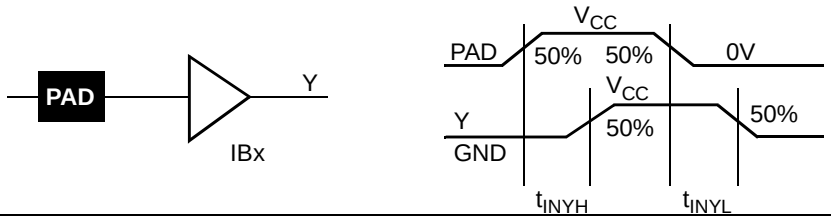
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 70°C)

Macro Type	Description	Max t_{DLH}	Max t_{DHL}	Max t_{ENZH}	Max t_{ENZL}	Units
OTB33PH	3.3V, PCI Output Current, High Slew Rate	2.4	2.2	2.6	2.7	ns
OTB33PN	3.3V, PCI Output Current, Nominal Slew Rate	2.9	2.7	3.1	3.3	ns
OTB33PL	3.3V, PCI Output Current, Low Slew Rate	3.5	3.4	3.7	3.9	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	3.4	3.8	3.6	4.3	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	4.3	4.5	4.5	5.1	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	4.9	6.3	5.1	6.8	ns
OTB25HH	2.5V, High Output Current, High Slew Rate	2.7	2.2	2.9	2.8	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate	3.5	3.2	3.7	3.8	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate	4.2	3.6	4.4	4.1	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate	3.9	4.9	4.1	5.4	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate	5.7	4.6	5.9	5.2	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate	7.1	6.0	7.4	6.5	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	6.0	1.9	6.2	2.4	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	5.9	2.8	6.1	3.4	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	5.9	4.3	6.1	4.9	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	9.2	2.7	9.4	3.2	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	9.2	3.8	9.4	4.3	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	9.2	5.4	9.4	5.9	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*
3. *t_{ENZH} = Enable-to-Pad, Z to HIGH*
4. *t_{ENZL} = Enable-to-Pad, Z to LOW*

Input Buffer Delays



Input Buffer Delays

(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	0.5	0.8	ns
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	0.8	0.8	ns
IB25LP	2.5V, CMOS Input Levels, Low Power	1.1	0.7	ns
IB25LPS	2.5V, CMOS Input Levels, Low Power	0.9	0.9	ns
IB33	3.3V, CMOS Input Levels, No Pull-up Resistor	0.9	0.6	ns
IB33S	3.3V, CMOS Input Levels, No Pull-up Resistor	1.2	0.5	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y HIGH*
2. *t_{INYL} = Input Pad-to-Y LOW*

Global Input Buffer Delays

(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
GL25	2.5V, CMOS Input Levels	1.9	1.6	ns
GL25S	2.5V, CMOS Input Levels	1.8	1.8	ns
GL25LP	2.5V, CMOS Input Levels	1.7	2.2	ns
GL25LPS	2.5V, CMOS Input Levels	1.9	1.9	ns
GL33	3.3V, CMOS Input Levels	1.9	1.6	ns
GL33S	3.3V, CMOS Input Levels	2.2	1.5	ns

Predicted Global Routing Delay*

(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (fully loaded row—32 inputs)	1.2	ns
t_{RCKL}	Input High to Low (fully loaded row—32 inputs)	1.1	ns
t_{RCKH}	Input Low to High (minimally loaded row—1 input)	0.9	ns
t_{RCKL}	Input High to Low (minimally loaded row—1 input)	0.9	ns

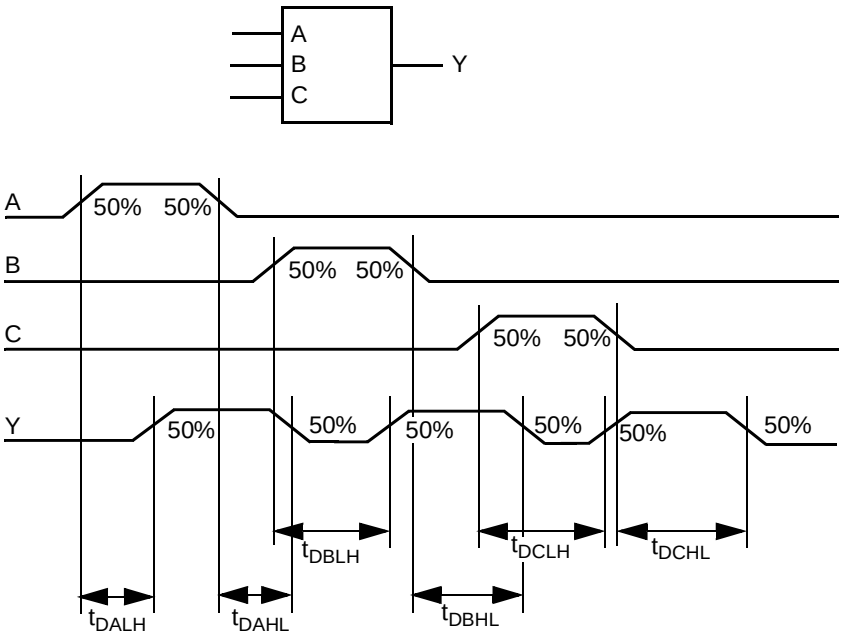
** The timing delay difference between tile locations is less than 15ps.*

Global Routing Skew

(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	0.3	ns
t_{RCKSHH}	Maximum Skew High to Low	0.3	ns

Module Delays



Sample Macrocell Library Listing

(Worst-Case Commercial Conditions, V_{DD} = 2.3V, T_J = 70° C)

Cell Name	Description	Maximum Intrinsic Delay	Minimum Setup/Hold	Units
NAND2	2-Input NAND	0.4		ns
AND2	2-Input AND	0.4		ns
NOR3	3-Input NOR	0.4		ns
MUX2L	2-1 Mux with Active Low Select	0.4		ns
OA21	2-Input OR into a 2-Input AND	0.4		ns
XOR2	2-Input Exclusive OR	0.3		ns
LDL	Active Low Latch (LH/HL)	D: 0.3/0.2	t_{setup} 0.5 t_{hold} 0.2	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)	CLK-Q: 0.4/0.4	t_{setup} 0.4 t_{hold} 0.2	ns

Note: *Assumes fanout of two.*

Slew Rates Measured at C = 10pF, Nominal Power Supplies and 25°C

Type	Trig. Lev.	Rising Edge	Slew Rate	Falling Edge	Slew Rate
		pS	V/nS	pS	V/nS
OB33PH	20%-60%	397	3.33	390	-3.38
OB33PN	20%-60%	463	2.85	450	-2.93
OB33PL	20%-60%	567	2.33	527	-2.51
OB33LH	20%-60%	467	2.83	700	-1.89
OB33LN	20%-60%	620	2.13	767	-1.72
OB33LL	20%-60%	813	1.62	1100	-1.20
OB25HH	20%-60%	750	1.33	310	-3.23
OB25HN	20%-60%	850	1.18	390	-2.56
OB25HL	20%-60%	1310	0.76	510	-1.96
OB25LH	20%-60%	793	1.26	430	-2.33
OB25LN	20%-60%	870	1.15	730	-1.37
OB25LL	20%-60%	1287	0.78	1037	-0.96
OB25LPHH	20%-60%	470	2.13	433	-2.31
OB25LPHN	20%-60%	533	1.81	527	-1.90
OB25LPHL	20%-60%	770	1.30	753	-1.33
OB25LPLH	20%-60%	597	1.68	707	-1.42
OB25LPLN	20%-60%	873	1.15	760	-1.32
OB25LPLL	20%-60%	1153	0.87	1563	-0.54

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 4). Table 3 on page 14 shows basic RAM and FIFO configurations. Simultaneous Read and Write to the same location must be done with care. On such accesses the DI bus is output to the DO bus.

Enclosed Timing Diagrams—SRAM Mode:

- Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Asynchronous RAM Write
- Asynchronous RAM Read, Address Controlled, RDB=0
- Asynchronous RAM Read, RDB Controlled
- Synchronous RAM Write
- Embedded Memory Specifications

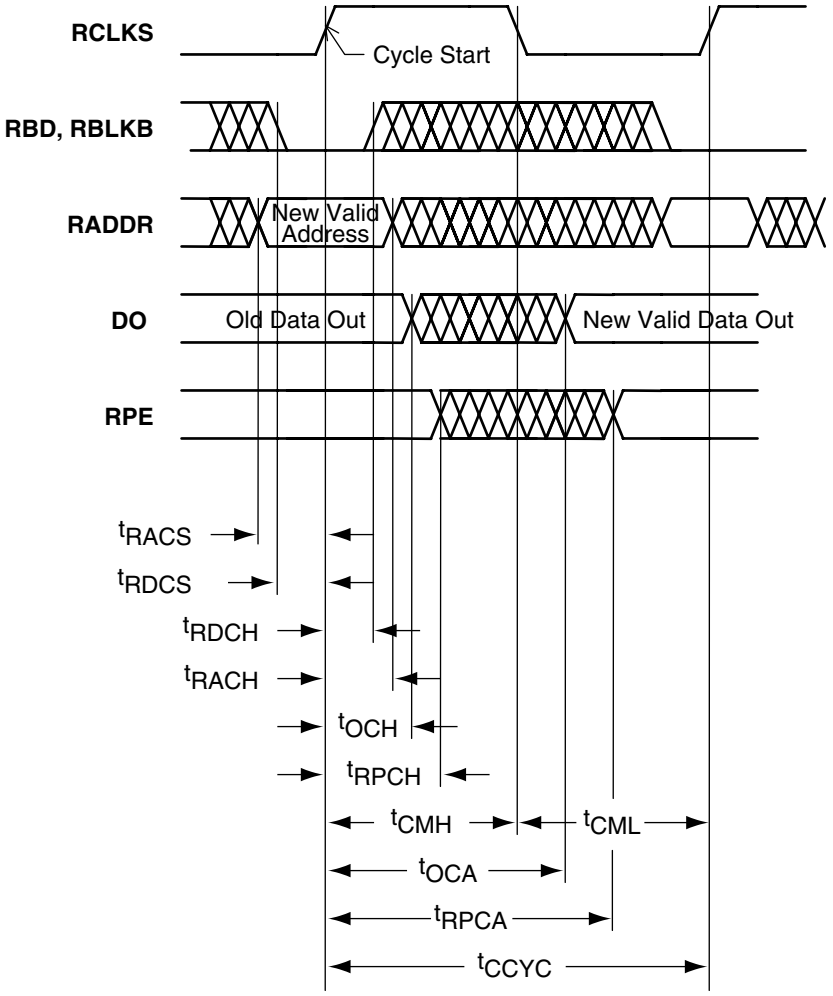
Note: *The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is thus nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.*

Table 4 • *Memory Block SRAM Interface Signals*

SRAM Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used on synchronization on write side
RCLKS	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	8	IN	Read address
RBLKB	1	IN	Negative true read block select
RDB	1	IN	Negative true read pulse
WADDR<0:7>	8	IN	Write address
WBLKB	1	IN	Negative true write block select
DI<0:8>	9	IN	Input data bits <0:8>, <8> can be used for parity in
WRB	1	IN	Negative true write pulse
DO<0:8>	9	OUT	Output data bits <0:8>, <8> can be used for parity out
RPE	1	OUT	Read parity error
WPE	1	OUT	Write parity error
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Note: *Not all signals shown are used in all modes.*

Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)

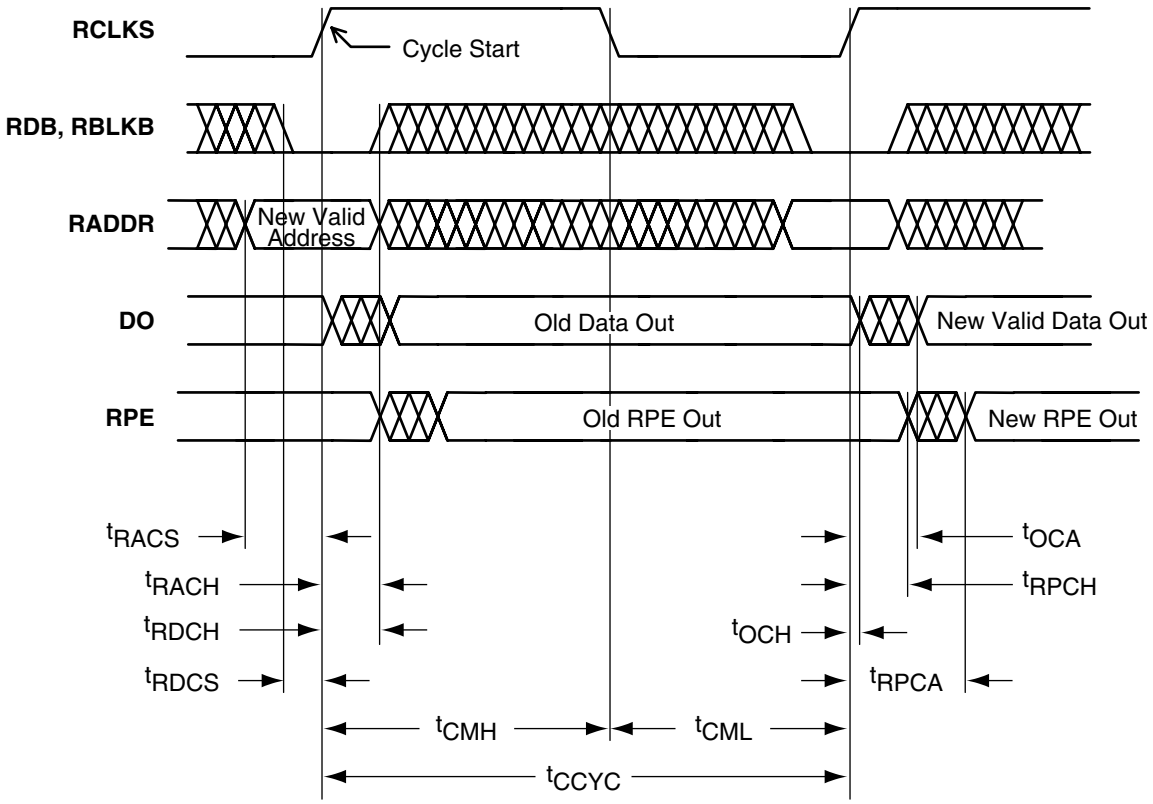


Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)

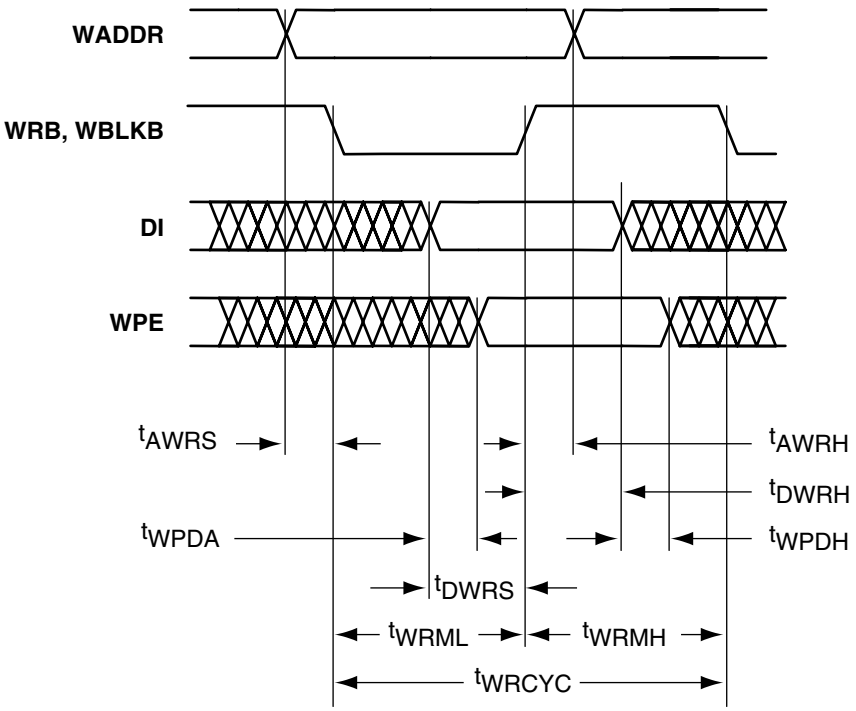


Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	

Asynchronous RAM Write

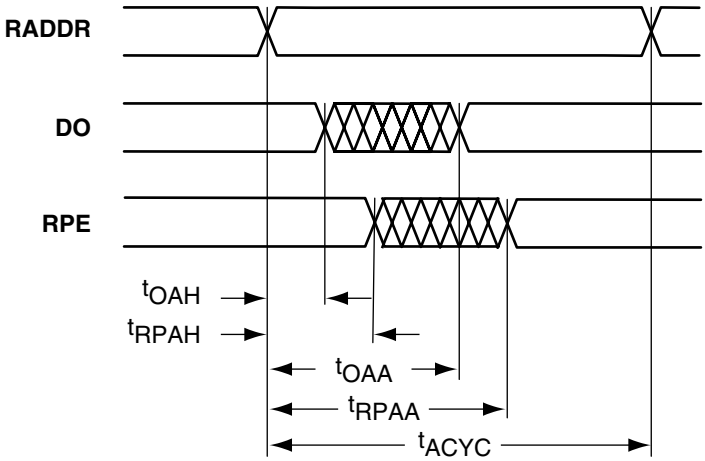


Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Asynchronous RAM Read, Address Controlled, RDB=0

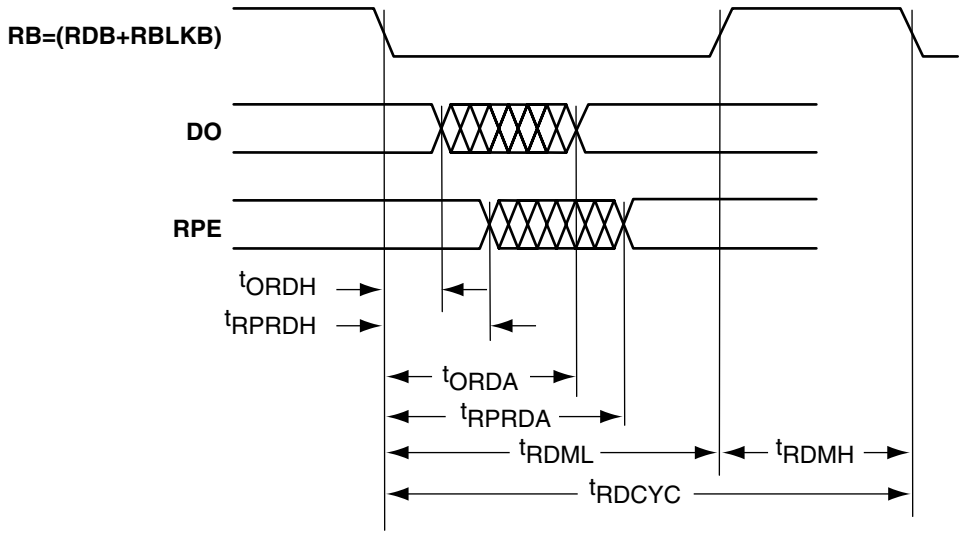


Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Asynchronous RAM Read, RDB Controlled

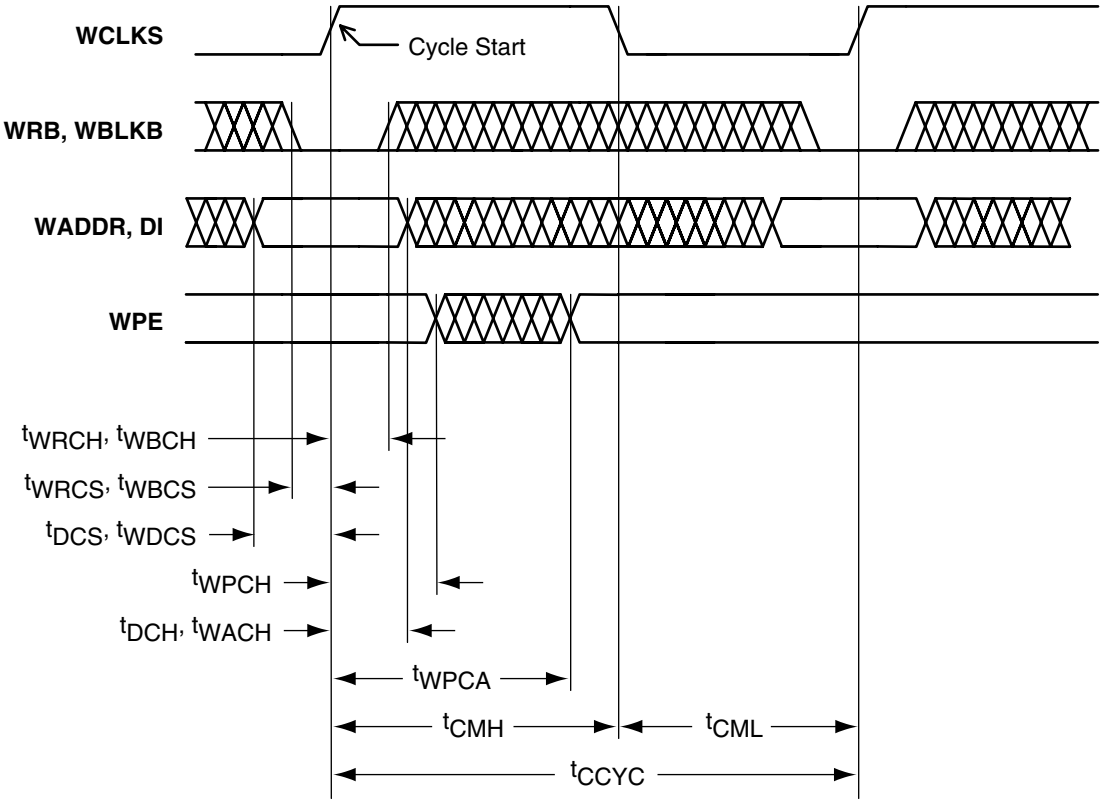


Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Synchronous RAM Write



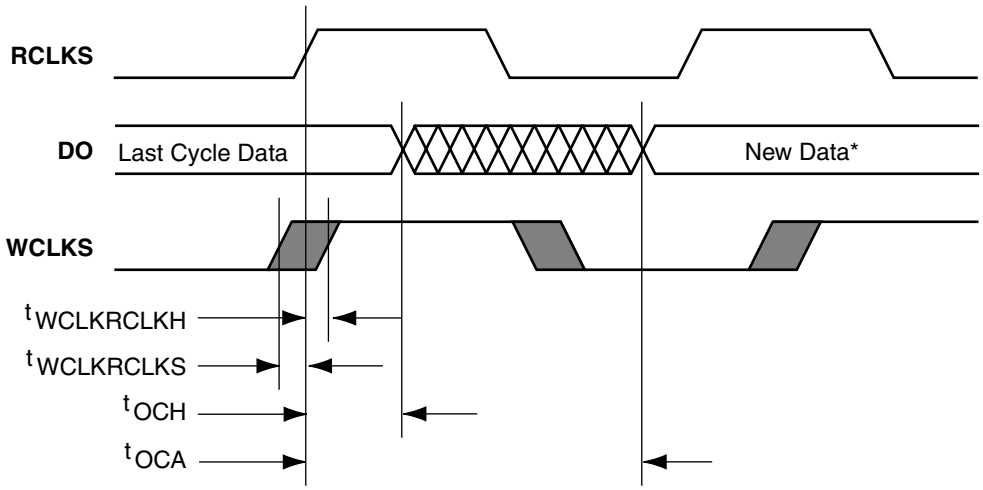
Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note: On simultaneous read and write accesses to the same location DI is output to DO.

Synchronous Write and Read to the Same Location



* New data is read if WCLKS ↑ occurs before setup time.
The data stored is read if WCLKS ↑ occurs after hold time.

Note: *The plot shows the normal operation status.*

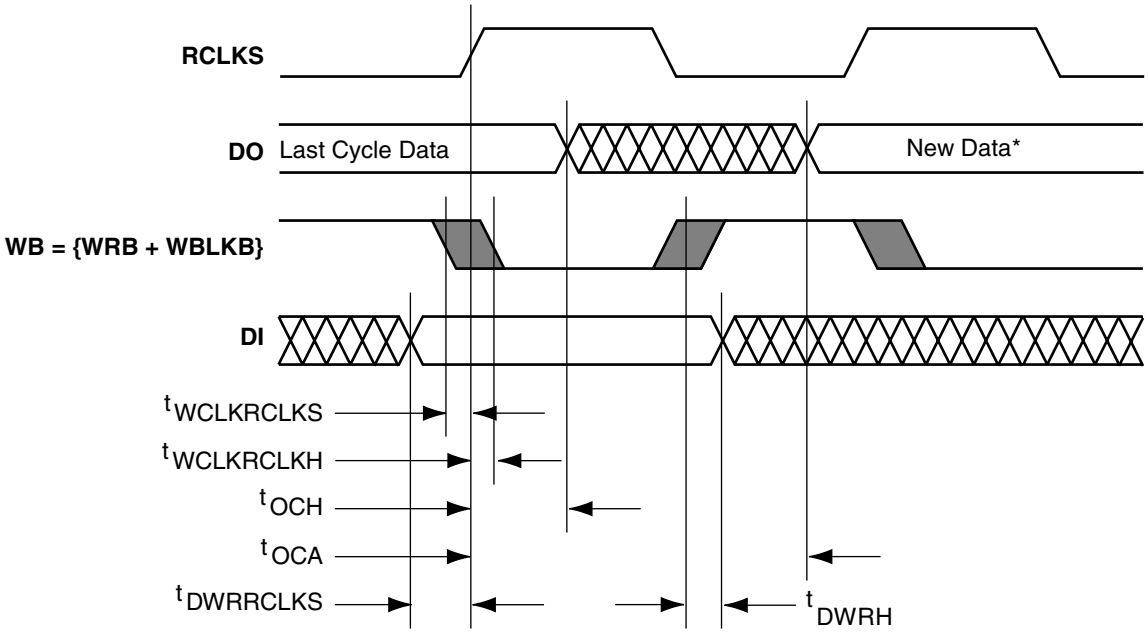
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write and Synchronous Read to the Same Location



* New data is read if WB ↓ occurs before setup time.
The stored data is read if WB ↓ occurs after hold time.

Note: *The plot shows the normal operation status.*

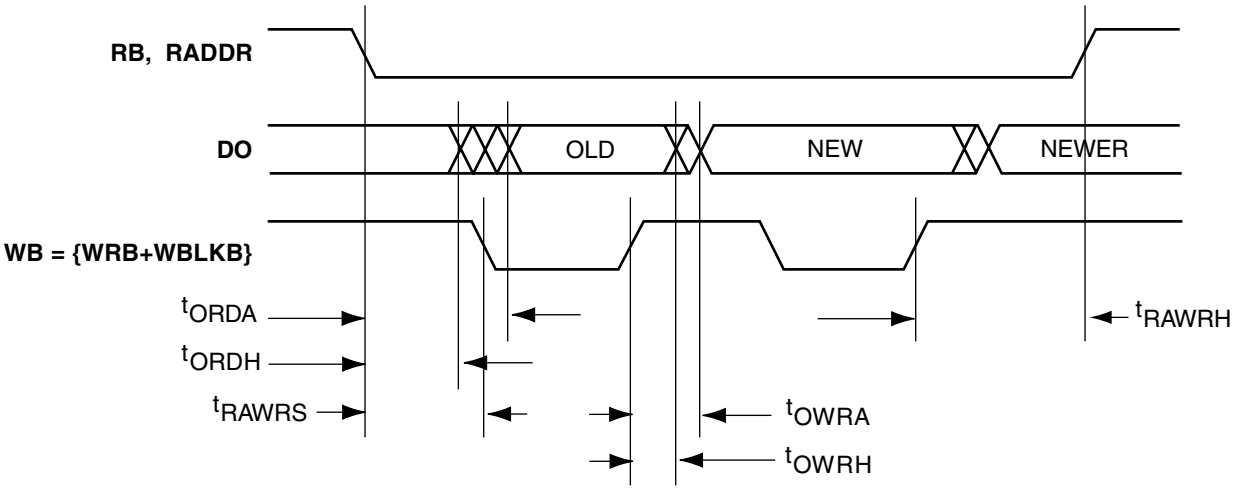
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

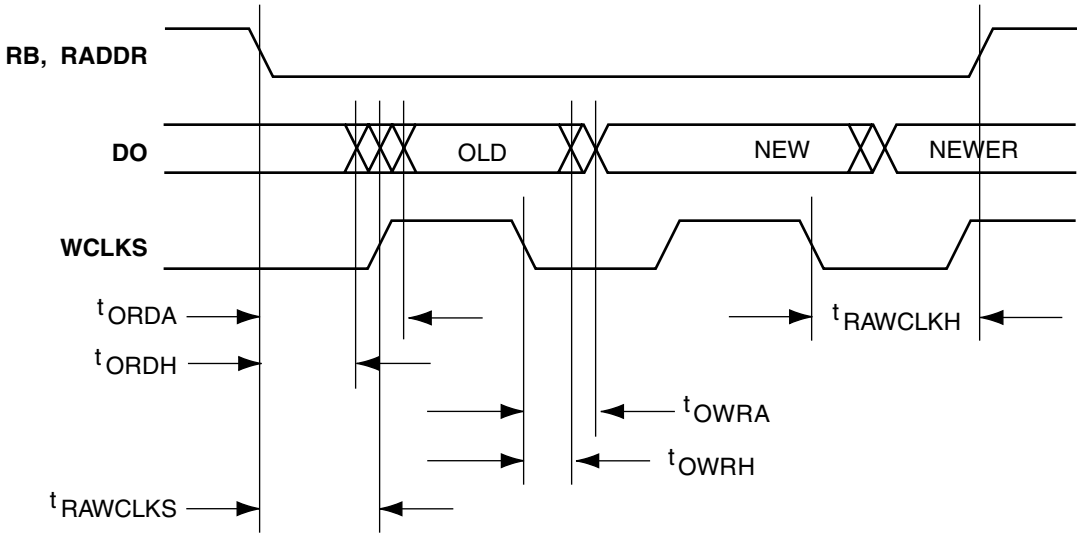
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WB ↑	3.0		ns	
OWRH	Old DO valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation or RAWRS will disturb access to the OLD data.*
3. *Violation of RAWRH will disturb access to the NEWER data.*

Synchronous Write and Asynchronous Read to the Same Location



Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WCLKS ↓	3.0		ns	
OWRH	Old DO valid from WCLKS ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLKS ↓	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation of RAWCLKS will disturb access to OLD data.*
3. *Violation of RAWCLKH will disturb access to NEWER data.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write (read) operation changes from inhibited to accepted after the read (write) signal which causes the transition from full (empty) to not full (empty) is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full (not empty) and ends 3 ns after the RB (WB) transition for slow cycles. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 5).

The timing diagram for write is shown in Figure 21 on page 47. The timing diagram for read is shown in Figure 22 on page 47. For basic RAM configurations, see Table 3 on page 14.

Enclosed Timing Diagrams – FIFO Mode:

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

Table 5 • Memory Block FIFO Interface Signals

FIFO Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used for synchronization on write side
RCLKS	1	IN	Read clock used for synchronization on read side
LEVEL <0:7>	8	IN	Direct configuration implements static flag logic
RBLKB	1	IN	Negative true read block select
RDB	1	IN	Negative true read pulse
RESET	1	IN	Negative true reset for FIFO pointers
WBLKB	1	IN	Negative true write block select
DI<0:8>	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	IN	Negative true write pulse
FULL, EMPTY	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	OUT	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	OUT	Output data bits <0:8>
RPE	1	OUT	Read parity error
WPE	1	OUT	Write parity error
LGDEP <0:2>	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

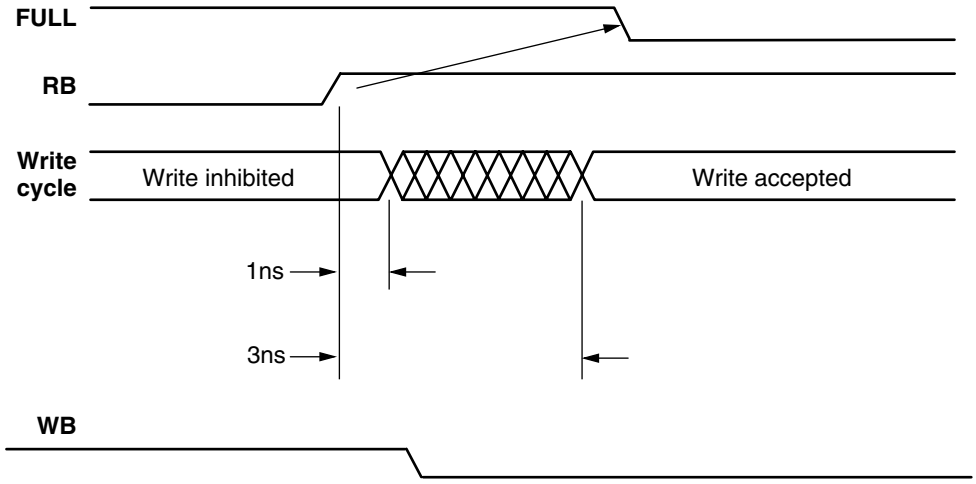


Figure 21 • *Write Timing Diagram*

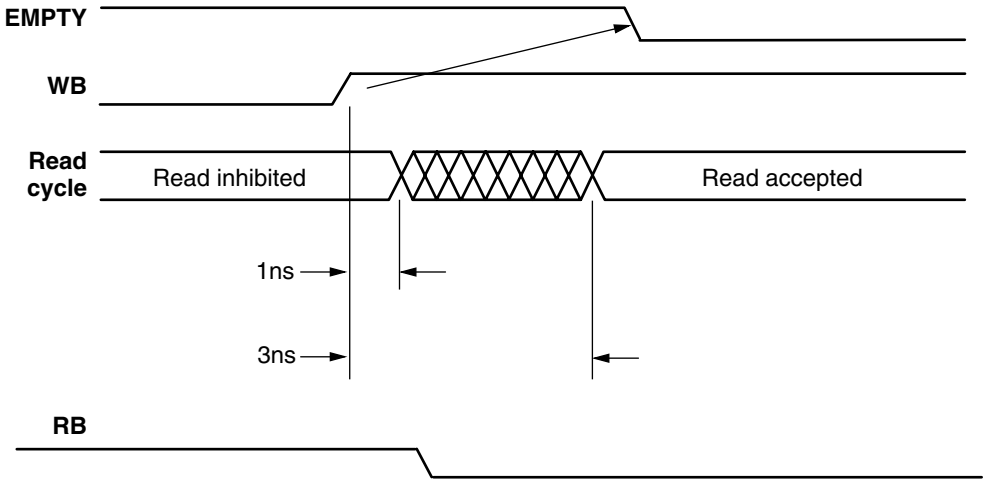
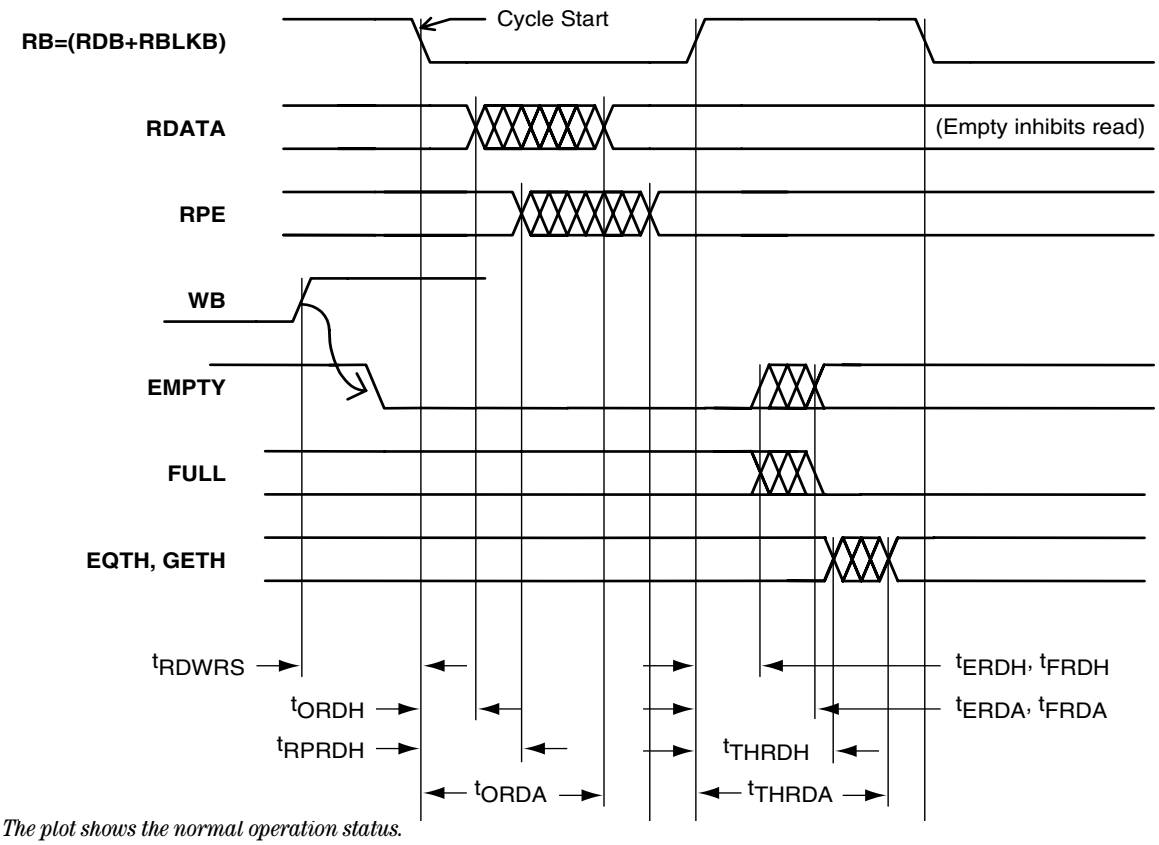


Figure 22 • *Read Timing Diagram*

Asynchronous FIFO Read



Note: The plot shows the normal operation status.

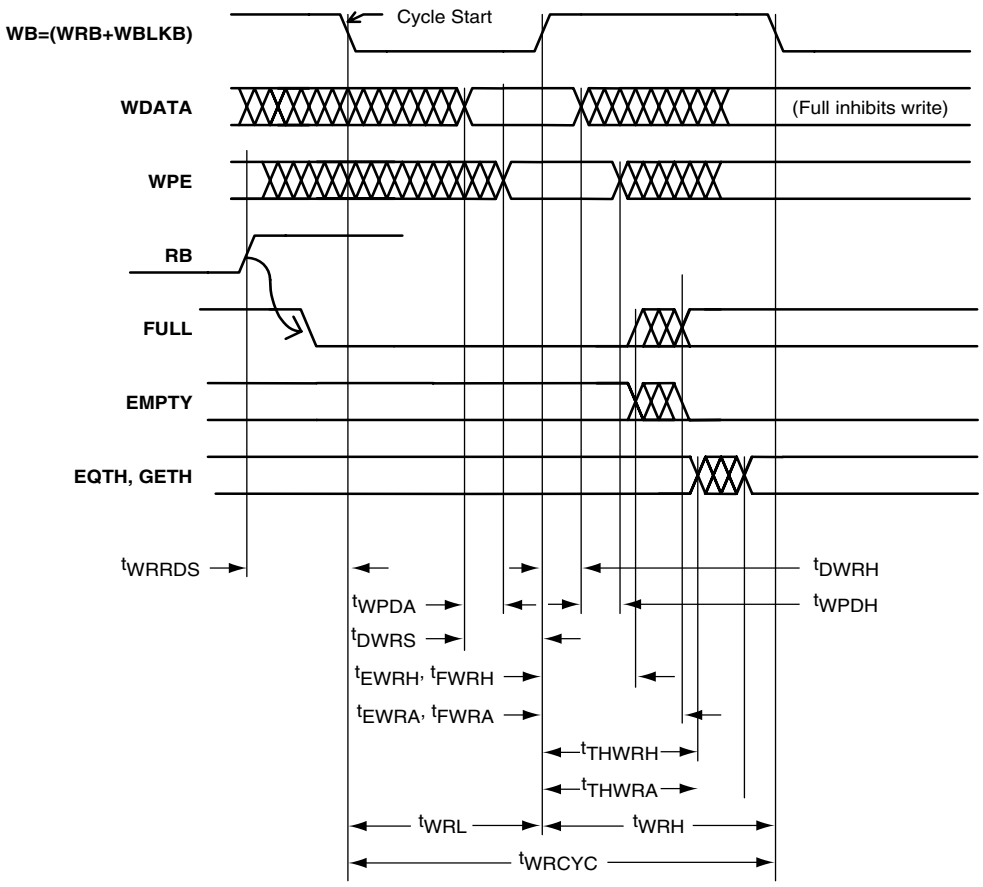
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA & FRDA = MAX (7.5 ns – RDL), 3.0 ns*
2. *At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns*

Asynchronous FIFO Write



Note: The plot shows the normal operation status.

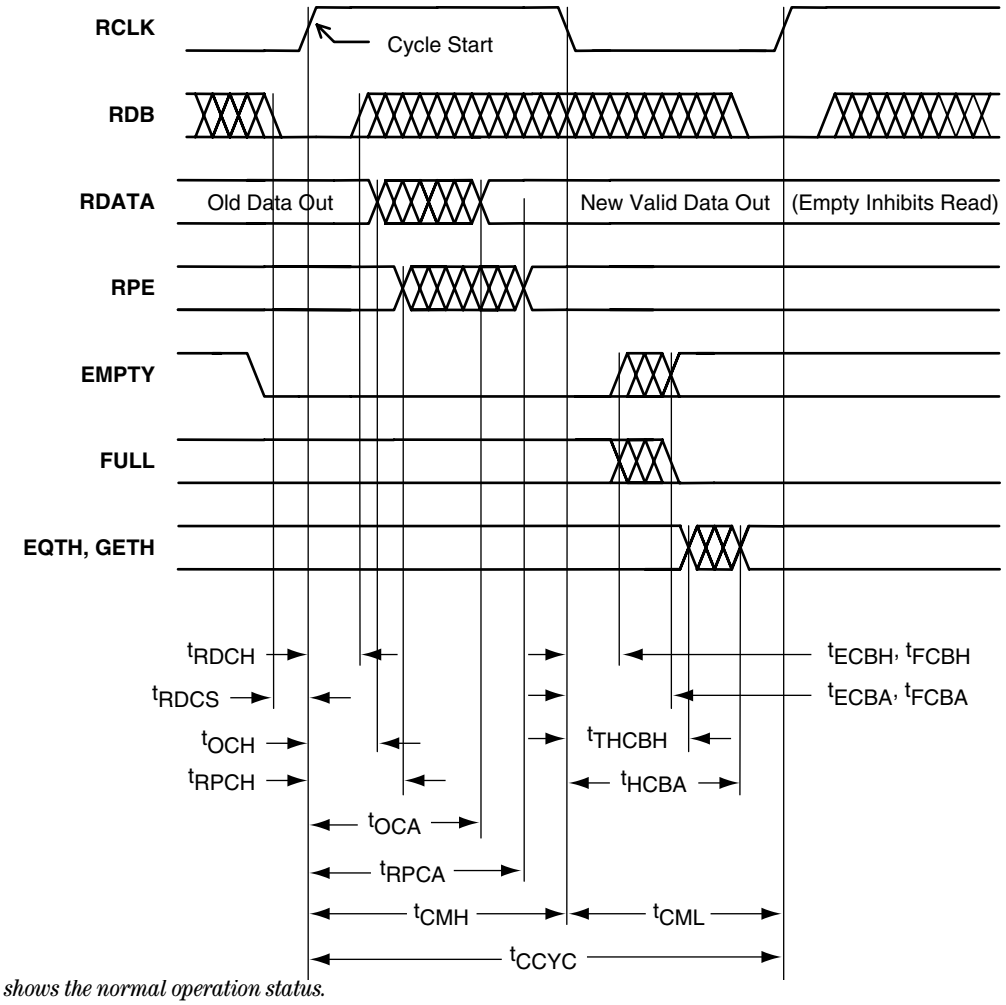
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. *At fast cycles, EWRA, FWRA = MAX (7.5 ns – WRL), 3.0 ns*
2. *At fast cycles, WRRDS (for enabling write) = MAX (7.5 ns – RDL), 3.0 ns*

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: The plot shows the normal operation status.

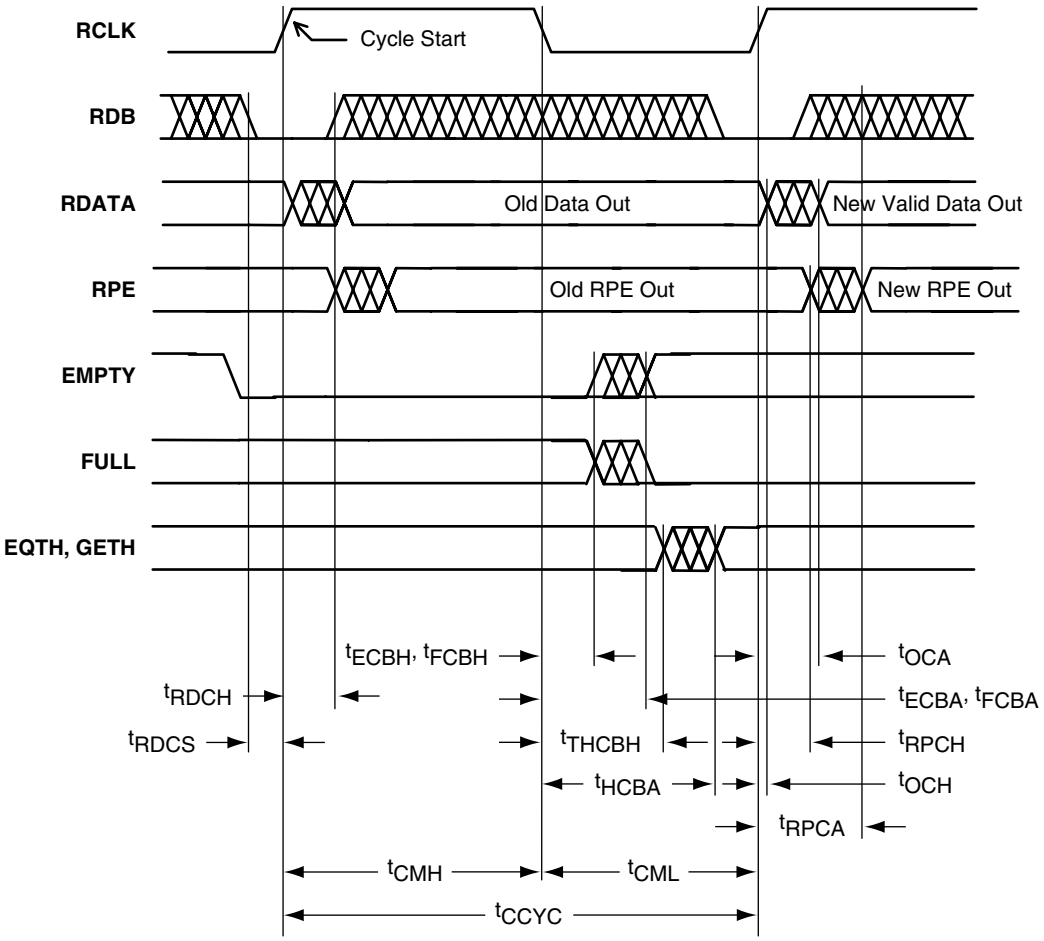
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX (7.5 ns – CMH), 3.0 ns

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: The plot shows the normal operation status.

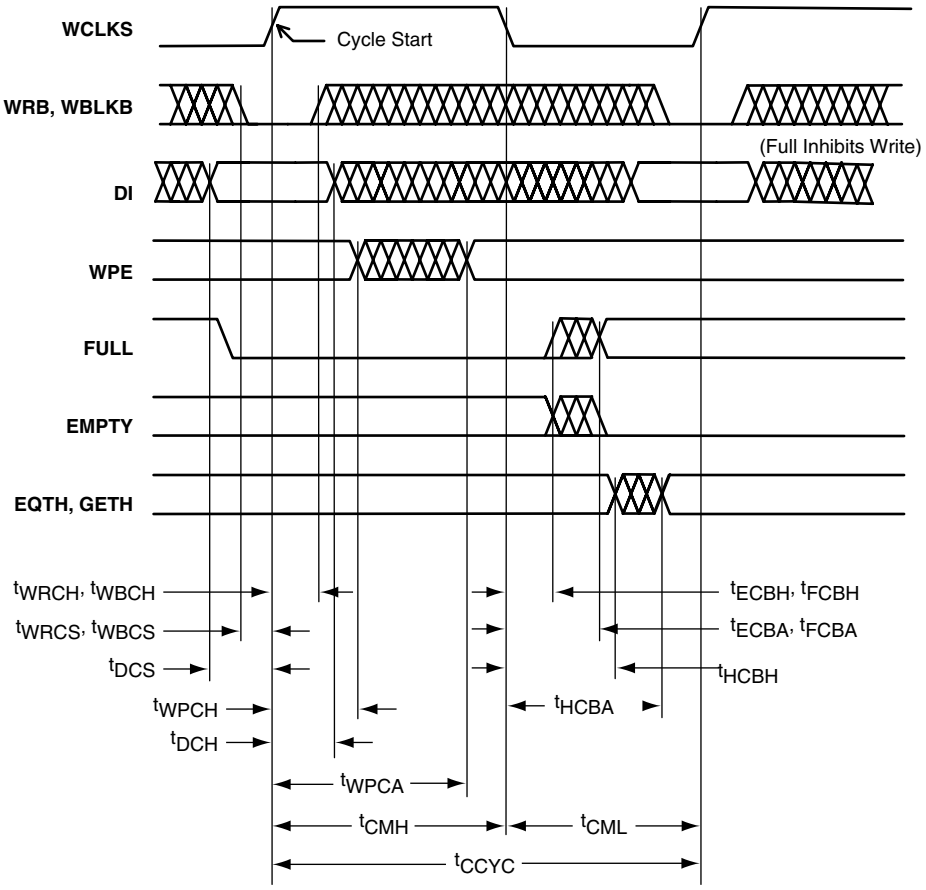
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX (7.5 ns – CMS), 3.0 ns

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

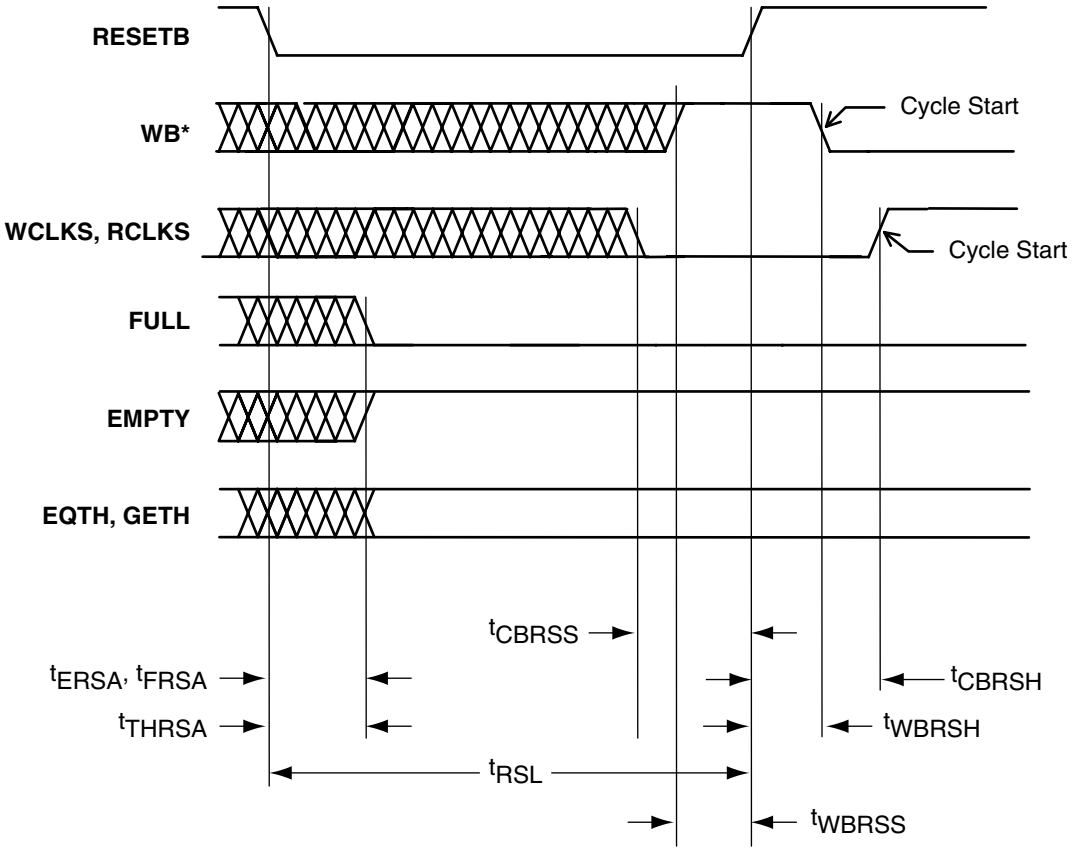
T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note:

1. *At fast cycles, ECBA & FCBA = MAX (7.5 ns – CMH), 3.0 ns*

FIFO Reset



Note: The plot shows the normal operation status.

T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only
CBRSS	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only
WBRSS	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only

Pin Description

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC products it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Input Pin**

Low skew input pin for clock or other global signals. Input only. This pin can be configured with a pull-up resistor.

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5V or 3.3V supply voltage.

V_{PP} **Programming Supply Pin**

This pin may be connected to any voltage between GND and 16.5V during normal operation, or it can be left unconnected. For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application note.

V_{PN} **Programming Supply Pin**

This pin may be connected to any voltage between GND and 13.8V during normal operation, or it can be left unconnected. For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application note.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry.

TCK **Test Clock**

Clock input pin for boundary scan.

TDI **Test Data In**

Serial input for boundary scan.

TDO **Test Data Out**

Serial output for boundary scan.

TRST **Test Reset Input**

Asynchronous, active low input pin for resetting boundary-scan circuitry.

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

NPECL **PECL Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **PECL Positive input**

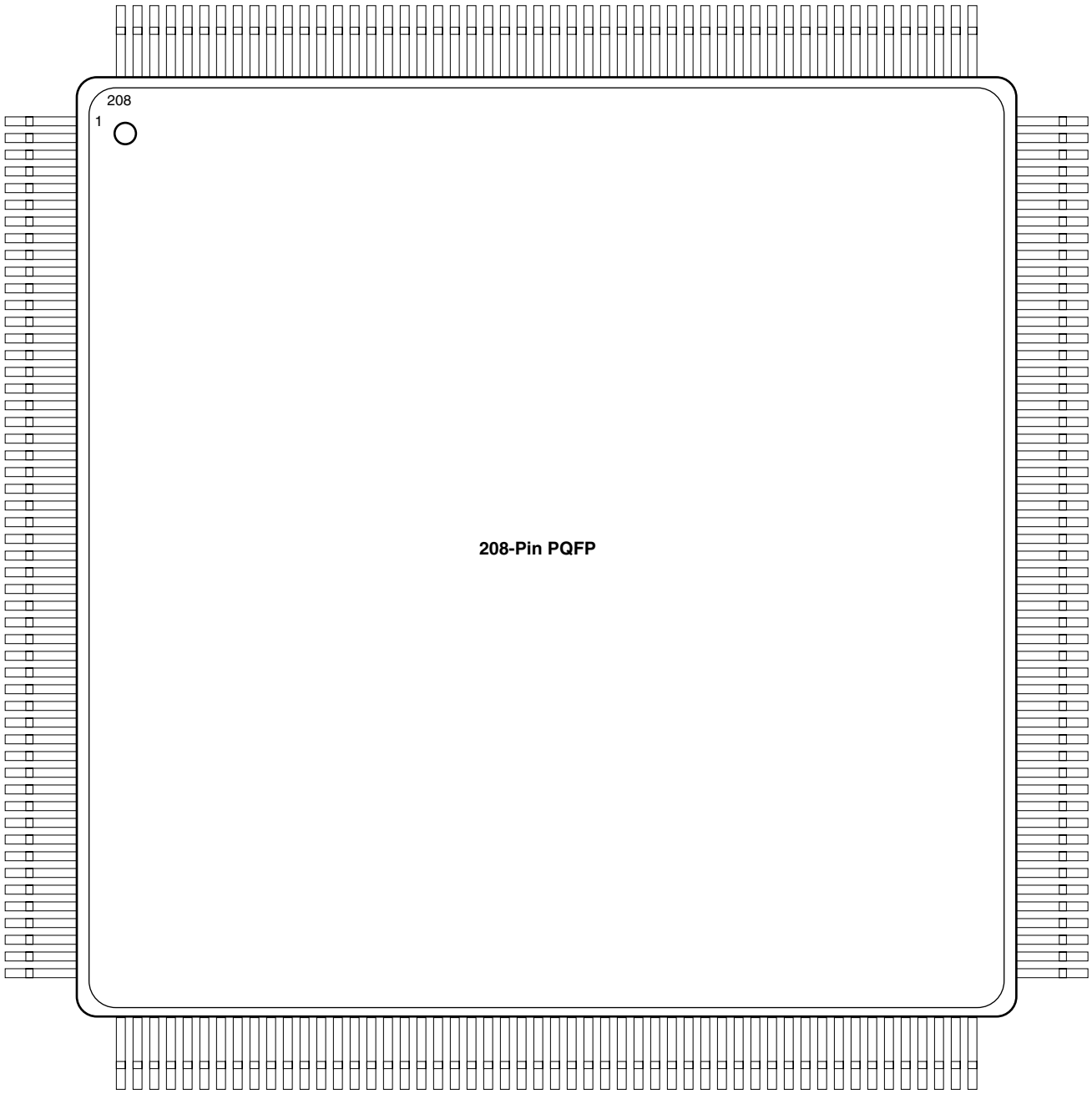
Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

AGND **PLL Power Ground**

Package Pin Assignments

208-Pin PQFP



208-Pin PQFP

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
1	GND	GND	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O
16	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
17	GND	GND	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O	I/O	I/O	I/O	I/O	I/O
24	GL	GL	GL	GL	GL	GL
25	AGND	AGND	AGND	AGND	AGND	AGND
26	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
27	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
28	PPECL	PPECL	PPECL	PPECL	PPECL	PPECL
29	GND	GND	GND	GND	GND	GND
30	GL	GL	GL	GL	GL	GL
31	I/O	I/O	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O	I/O	I/O
36	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
37	I/O	I/O	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O	I/O	I/O
71	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
79	I/O	I/O	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O	I/O	I/O
88	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
89	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O	I/O	I/O
101	TCK	TCK	TCK	TCK	TCK	TCK
102	TDI	TDI	TDI	TDI	TDI	TDI
103	TMS	TMS	TMS	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
105	GND	GND	GND	GND	GND	GND
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO	TDO	TDO	TDO
109	TRST	TRST	TRST	TRST	TRST	TRST
110	RCK	RCK	RCK	RCK	RCK	RCK
111	I/O	I/O	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
118	I/O	I/O	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O	I/O	I/O
126	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
127	I/O	I/O	I/O	I/O	I/O	I/O
128	GL	GL	GL	GL	GL	GL
129	PPECL	PPECL	PPECL	PPECL	PPECL	PPECL
130	GND	GND	GND	GND	GND	GND
131	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
132	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
133	AGND	AGND	AGND	AGND	AGND	AGND
134	GL	GL	GL	GL	GL	GL
135	I/O	I/O	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND	GND	GND
142	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
143	I/O	I/O	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND	GND	GND

208-Pin PQFP (Continued)

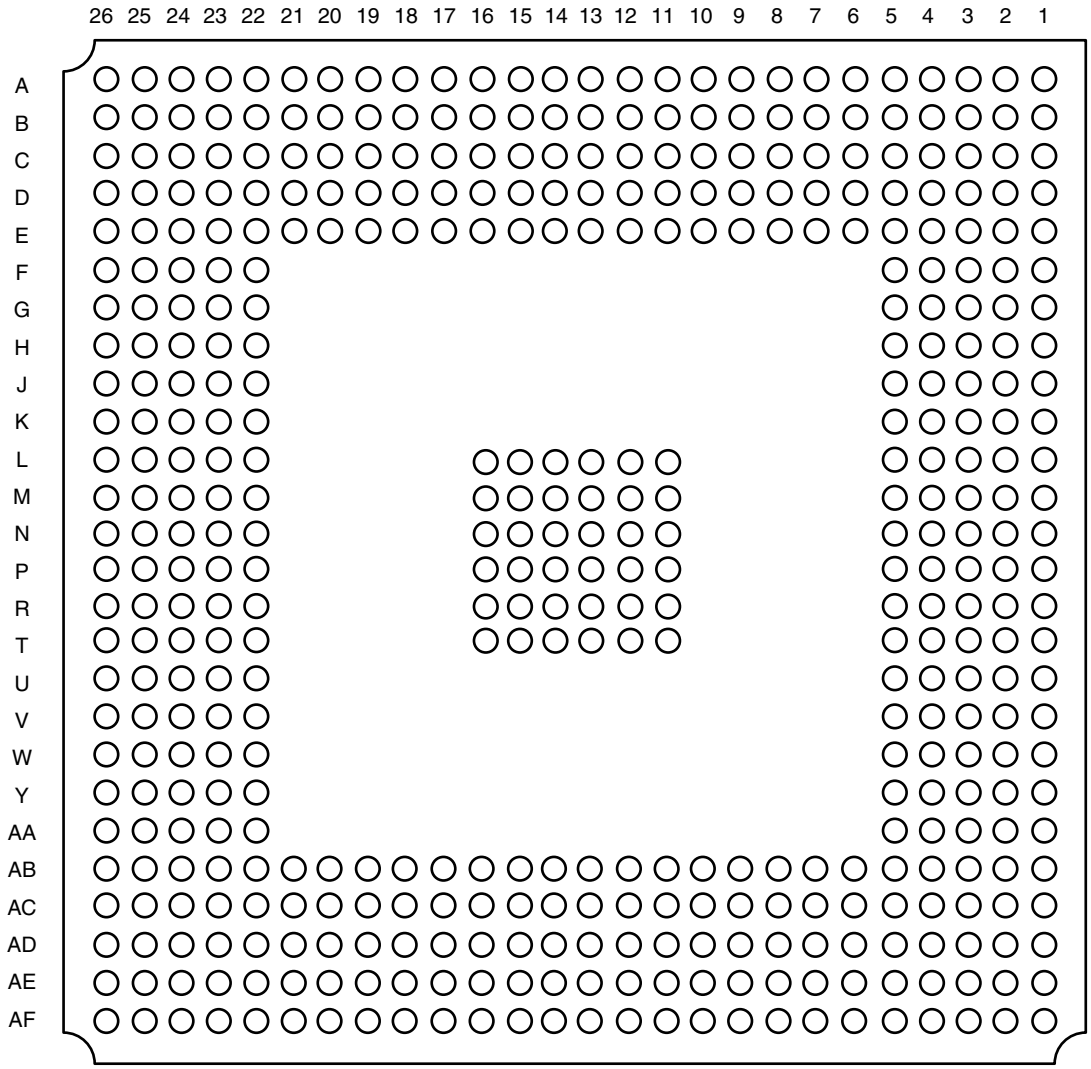
Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND	GND	GND
163	I/O	I/O	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
172	I/O	I/O	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O	I/O	I/O
184	I/O	I/O	I/O	I/O	I/O	I/O
185	I/O	I/O	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
188	I/O	I/O	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND	GND	GND

208-Pin PQFP (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
196	I/O	I/O	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

Package Pin Assignments (Continued)

456-Pin PBGA (Bottom View)



456-Pin PBGA

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
A1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A3	NC	NC	I/O	I/O	I/O	I/O
A4	NC	NC	I/O	I/O	I/O	I/O
A5	NC	NC	I/O	I/O	I/O	I/O
A6	NC	NC	I/O	I/O	I/O	I/O
A7	NC	NC	I/O	I/O	I/O	I/O
A8	I/O	I/O	I/O	I/O	I/O	I/O
A9	I/O	I/O	I/O	I/O	I/O	I/O
A10	I/O	I/O	I/O	I/O	I/O	I/O
A11	I/O	I/O	I/O	I/O	I/O	I/O
A12	I/O	I/O	I/O	I/O	I/O	I/O
A13	I/O	I/O	I/O	I/O	I/O	I/O
A14	I/O	I/O	I/O	I/O	I/O	I/O
A15	I/O	I/O	I/O	I/O	I/O	I/O
A16	I/O	I/O	I/O	I/O	I/O	I/O
A17	I/O	I/O	I/O	I/O	I/O	I/O
A18	I/O	I/O	I/O	I/O	I/O	I/O
A19	I/O	I/O	I/O	I/O	I/O	I/O
A20	NC	NC	I/O	I/O	I/O	I/O
A21	NC	NC	I/O	I/O	I/O	I/O
A22	NC	NC	I/O	I/O	I/O	I/O
A23	NC	NC	I/O	I/O	I/O	I/O
A24	NC	NC	I/O	I/O	I/O	I/O
A25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B3	NC	NC	NC	I/O	I/O	I/O
B4	NC	NC	I/O	I/O	I/O	I/O
B5	NC	NC	I/O	I/O	I/O	I/O
B6	NC	NC	I/O	I/O	I/O	I/O
B7	NC	NC	I/O	I/O	I/O	I/O
B8	I/O	I/O	I/O	I/O	I/O	I/O
B9	I/O	I/O	I/O	I/O	I/O	I/O
B10	I/O	I/O	I/O	I/O	I/O	I/O
B11	I/O	I/O	I/O	I/O	I/O	I/O
B12	I/O	I/O	I/O	I/O	I/O	I/O
B13	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
B14	I/O	I/O	I/O	I/O	I/O	I/O
B15	I/O	I/O	I/O	I/O	I/O	I/O
B16	I/O	I/O	I/O	I/O	I/O	I/O
B17	I/O	I/O	I/O	I/O	I/O	I/O
B18	I/O	I/O	I/O	I/O	I/O	I/O
B19	I/O	I/O	I/O	I/O	I/O	I/O
B20	NC	NC	I/O	I/O	I/O	I/O
B21	NC	NC	I/O	I/O	I/O	I/O
B22	NC	NC	I/O	I/O	I/O	I/O
B23	NC	NC	I/O	I/O	I/O	I/O
B24	NC	NC	I/O	I/O	I/O	I/O
B25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C2	NC	I/O	I/O	I/O	I/O	I/O
C3	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C4	NC	NC	NC	I/O	I/O	I/O
C5	NC	NC	I/O	I/O	I/O	I/O
C6	NC	NC	I/O	I/O	I/O	I/O
C7	I/O	I/O	I/O	I/O	I/O	I/O
C8	I/O	I/O	I/O	I/O	I/O	I/O
C9	I/O	I/O	I/O	I/O	I/O	I/O
C10	I/O	I/O	I/O	I/O	I/O	I/O
C11	I/O	I/O	I/O	I/O	I/O	I/O
C12	I/O	I/O	I/O	I/O	I/O	I/O
C13	I/O	I/O	I/O	I/O	I/O	I/O
C14	I/O	I/O	I/O	I/O	I/O	I/O
C15	I/O	I/O	I/O	I/O	I/O	I/O
C16	I/O	I/O	I/O	I/O	I/O	I/O
C17	I/O	I/O	I/O	I/O	I/O	I/O
C18	I/O	I/O	I/O	I/O	I/O	I/O
C19	I/O	I/O	I/O	I/O	I/O	I/O
C20	I/O	I/O	I/O	I/O	I/O	I/O
C21	NC	NC	I/O	I/O	I/O	I/O
C22	NC	NC	I/O	I/O	I/O	I/O
C23	NC	NC	I/O	I/O	I/O	I/O
C24	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C25	NC	NC	NC	I/O	I/O	I/O
C26	NC	NC	NC	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
D1	NC	NC	NC	I/O	I/O	I/O
D2	NC	NC	NC	I/O	I/O	I/O
D3	NC	I/O	I/O	I/O	I/O	I/O
D4	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
D5	NC	NC	I/O	I/O	I/O	I/O
D6	NC	NC	I/O	I/O	I/O	I/O
D7	I/O	I/O	I/O	I/O	I/O	I/O
D8	I/O	I/O	I/O	I/O	I/O	I/O
D9	I/O	I/O	I/O	I/O	I/O	I/O
D10	I/O	I/O	I/O	I/O	I/O	I/O
D11	I/O	I/O	I/O	I/O	I/O	I/O
D12	I/O	I/O	I/O	I/O	I/O	I/O
D13	I/O	I/O	I/O	I/O	I/O	I/O
D14	I/O	I/O	I/O	I/O	I/O	I/O
D15	I/O	I/O	I/O	I/O	I/O	I/O
D16	I/O	I/O	I/O	I/O	I/O	I/O
D17	I/O	I/O	I/O	I/O	I/O	I/O
D18	I/O	I/O	I/O	I/O	I/O	I/O
D19	I/O	I/O	I/O	I/O	I/O	I/O
D20	I/O	I/O	I/O	I/O	I/O	I/O
D21	I/O	I/O	I/O	I/O	I/O	I/O
D22	NC	NC	I/O	I/O	I/O	I/O
D23	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
D24	NC	I/O	I/O	I/O	I/O	I/O
D25	NC	NC	NC	I/O	I/O	I/O
D26	NC	NC	NC	I/O	I/O	I/O
E1	NC	I/O	I/O	I/O	I/O	I/O
E2	NC	I/O	I/O	I/O	I/O	I/O
E3	NC	I/O	I/O	I/O	I/O	I/O
E4	NC	I/O	I/O	I/O	I/O	I/O
E5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E6	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E8	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E9	I/O	I/O	I/O	I/O	I/O	I/O
E10	I/O	I/O	I/O	I/O	I/O	I/O
E11	I/O	I/O	I/O	I/O	I/O	I/O
E12	I/O	I/O	I/O	I/O	I/O	I/O
E13	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
E14	I/O	I/O	I/O	I/O	I/O	I/O
E15	I/O	I/O	I/O	I/O	I/O	I/O
E16	I/O	I/O	I/O	I/O	I/O	I/O
E17	I/O	I/O	I/O	I/O	I/O	I/O
E18	I/O	I/O	I/O	I/O	I/O	I/O
E19	I/O	I/O	I/O	I/O	I/O	I/O
E20	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E21	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E23	NC	I/O	I/O	I/O	I/O	I/O
E24	NC	I/O	I/O	I/O	I/O	I/O
E25	NC	I/O	I/O	I/O	I/O	I/O
E26	NC	I/O	I/O	I/O	I/O	I/O
F1	NC	I/O	I/O	I/O	I/O	I/O
F2	NC	I/O	I/O	I/O	I/O	I/O
F3	NC	I/O	I/O	I/O	I/O	I/O
F4	NC	I/O	I/O	I/O	I/O	I/O
F5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F23	NC	I/O	I/O	I/O	I/O	I/O
F24	NC	I/O	I/O	I/O	I/O	I/O
F25	NC	I/O	I/O	I/O	I/O	I/O
F26	NC	I/O	I/O	I/O	I/O	I/O
G1	I/O	I/O	I/O	I/O	I/O	I/O
G2	I/O	I/O	I/O	I/O	I/O	I/O
G3	NC	I/O	I/O	I/O	I/O	I/O
G4	NC	I/O	I/O	I/O	I/O	I/O
G5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G23	NC	I/O	I/O	I/O	I/O	I/O
G24	NC	I/O	I/O	I/O	I/O	I/O
G25	NC	I/O	I/O	I/O	I/O	I/O
G26	I/O	I/O	I/O	I/O	I/O	I/O
H1	I/O	I/O	I/O	I/O	I/O	I/O
H2	I/O	I/O	I/O	I/O	I/O	I/O
H3	I/O	I/O	I/O	I/O	I/O	I/O
H4	I/O	I/O	I/O	I/O	I/O	I/O
H5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
H23	I/O	I/O	I/O	I/O	I/O	I/O
H24	I/O	I/O	I/O	I/O	I/O	I/O
H25	I/O	I/O	I/O	I/O	I/O	I/O
H26	I/O	I/O	I/O	I/O	I/O	I/O
J1	I/O	I/O	I/O	I/O	I/O	I/O
J2	I/O	I/O	I/O	I/O	I/O	I/O
J3	I/O	I/O	I/O	I/O	I/O	I/O
J4	I/O	I/O	I/O	I/O	I/O	I/O
J5	I/O	I/O	I/O	I/O	I/O	I/O
J22	I/O	I/O	I/O	I/O	I/O	I/O
J23	I/O	I/O	I/O	I/O	I/O	I/O
J24	I/O	I/O	I/O	I/O	I/O	I/O
J25	I/O	I/O	I/O	I/O	I/O	I/O
J26	I/O	I/O	I/O	I/O	I/O	I/O
K1	I/O	I/O	I/O	I/O	I/O	I/O
K2	I/O	I/O	I/O	I/O	I/O	I/O
K3	I/O	I/O	I/O	I/O	I/O	I/O
K4	I/O	I/O	I/O	I/O	I/O	I/O
K5	I/O	I/O	I/O	I/O	I/O	I/O
K22	I/O	I/O	I/O	I/O	I/O	I/O
K23	I/O	I/O	I/O	I/O	I/O	I/O
K24	I/O	I/O	I/O	I/O	I/O	I/O
K25	I/O	I/O	I/O	I/O	I/O	I/O
K26	I/O	I/O	I/O	I/O	I/O	I/O
L1	I/O	I/O	I/O	I/O	I/O	I/O
L2	I/O	I/O	I/O	I/O	I/O	I/O
L3	I/O	I/O	I/O	I/O	I/O	I/O
L4	I/O	I/O	I/O	I/O	I/O	I/O
L5	I/O	I/O	I/O	I/O	I/O	I/O
L11	GND	GND	GND	GND	GND	GND
L12	GND	GND	GND	GND	GND	GND
L13	GND	GND	GND	GND	GND	GND
L14	GND	GND	GND	GND	GND	GND
L15	GND	GND	GND	GND	GND	GND
L16	GND	GND	GND	GND	GND	GND
L22	I/O	I/O	I/O	I/O	I/O	I/O
L23	I/O	I/O	I/O	I/O	I/O	I/O
L24	I/O	I/O	I/O	I/O	I/O	I/O
L25	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
L26	I/O	I/O	I/O	I/O	I/O	I/O
M1	GL	GL	GL	GL	GL	GL
M2	GL	GL	GL	GL	GL	GL
M3	I/O	I/O	I/O	I/O	I/O	I/O
M4	I/O	I/O	I/O	I/O	I/O	I/O
M5	I/O	I/O	I/O	I/O	I/O	I/O
M11	GND	GND	GND	GND	GND	GND
M12	GND	GND	GND	GND	GND	GND
M13	GND	GND	GND	GND	GND	GND
M14	GND	GND	GND	GND	GND	GND
M15	GND	GND	GND	GND	GND	GND
M16	GND	GND	GND	GND	GND	GND
M22	GL	GL	GL	GL	GL	GL
M23	I/O	I/O	I/O	I/O	I/O	I/O
M24	I/O	I/O	I/O	I/O	I/O	I/O
M25	I/O	I/O	I/O	I/O	I/O	I/O
M26	I/O	I/O	I/O	I/O	I/O	I/O
N1	I/O	I/O	I/O	I/O	I/O	I/O
N2	I/O	I/O	I/O	I/O	I/O	I/O
N3	AGND	AGND	AGND	AGND	AGND	AGND
N4	PPECL	PPECL	PPECL	PPECL	PPECL	PPECL
N5	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
N11	GND	GND	GND	GND	GND	GND
N12	GND	GND	GND	GND	GND	GND
N13	GND	GND	GND	GND	GND	GND
N14	GND	GND	GND	GND	GND	GND
N15	GND	GND	GND	GND	GND	GND
N16	GND	GND	GND	GND	GND	GND
N22	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
N23	GL	GL	GL	GL	GL	GL
N24	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
N25	I/O	I/O	I/O	I/O	I/O	I/O
N26	AGND	AGND	AGND	AGND	AGND	AGND
P1	I/O	I/O	I/O	I/O	I/O	I/O
P2	I/O	I/O	I/O	I/O	I/O	I/O
P3	I/O	I/O	I/O	I/O	I/O	I/O
P4	I/O	I/O	I/O	I/O	I/O	I/O
P5	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
P11	GND	GND	GND	GND	GND	GND

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
P12	GND	GND	GND	GND	GND	GND
P13	GND	GND	GND	GND	GND	GND
P14	GND	GND	GND	GND	GND	GND
P15	GND	GND	GND	GND	GND	GND
P16	GND	GND	GND	GND	GND	GND
P22	I/O	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O	I/O
P26	PPECL	PPECL	PPECL	PPECL	PPECL	PPECL
R1	I/O	I/O	I/O	I/O	I/O	I/O
R2	I/O	I/O	I/O	I/O	I/O	I/O
R3	I/O	I/O	I/O	I/O	I/O	I/O
R4	I/O	I/O	I/O	I/O	I/O	I/O
R5	I/O	I/O	I/O	I/O	I/O	I/O
R11	GND	GND	GND	GND	GND	GND
R12	GND	GND	GND	GND	GND	GND
R13	GND	GND	GND	GND	GND	GND
R14	GND	GND	GND	GND	GND	GND
R15	GND	GND	GND	GND	GND	GND
R16	GND	GND	GND	GND	GND	GND
R22	I/O	I/O	I/O	I/O	I/O	I/O
R23	I/O	I/O	I/O	I/O	I/O	I/O
R24	I/O	I/O	I/O	I/O	I/O	I/O
R25	I/O	I/O	I/O	I/O	I/O	I/O
R26	I/O	I/O	I/O	I/O	I/O	I/O
T1	I/O	I/O	I/O	I/O	I/O	I/O
T2	I/O	I/O	I/O	I/O	I/O	I/O
T3	I/O	I/O	I/O	I/O	I/O	I/O
T4	I/O	I/O	I/O	I/O	I/O	I/O
T5	I/O	I/O	I/O	I/O	I/O	I/O
T11	GND	GND	GND	GND	GND	GND
T12	GND	GND	GND	GND	GND	GND
T13	GND	GND	GND	GND	GND	GND
T14	GND	GND	GND	GND	GND	GND
T15	GND	GND	GND	GND	GND	GND
T16	GND	GND	GND	GND	GND	GND
T22	I/O	I/O	I/O	I/O	I/O	I/O
T23	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
T24	I/O	I/O	I/O	I/O	I/O	I/O
T25	I/O	I/O	I/O	I/O	I/O	I/O
T26	I/O	I/O	I/O	I/O	I/O	I/O
U1	I/O	I/O	I/O	I/O	I/O	I/O
U2	I/O	I/O	I/O	I/O	I/O	I/O
U3	I/O	I/O	I/O	I/O	I/O	I/O
U4	I/O	I/O	I/O	I/O	I/O	I/O
U5	I/O	I/O	I/O	I/O	I/O	I/O
U22	I/O	I/O	I/O	I/O	I/O	I/O
U23	I/O	I/O	I/O	I/O	I/O	I/O
U24	I/O	I/O	I/O	I/O	I/O	I/O
U25	I/O	I/O	I/O	I/O	I/O	I/O
U26	I/O	I/O	I/O	I/O	I/O	I/O
V1	I/O	I/O	I/O	I/O	I/O	I/O
V2	I/O	I/O	I/O	I/O	I/O	I/O
V3	I/O	I/O	I/O	I/O	I/O	I/O
V4	I/O	I/O	I/O	I/O	I/O	I/O
V5	I/O	I/O	I/O	I/O	I/O	I/O
V22	I/O	I/O	I/O	I/O	I/O	I/O
V23	I/O	I/O	I/O	I/O	I/O	I/O
V24	I/O	I/O	I/O	I/O	I/O	I/O
V25	I/O	I/O	I/O	I/O	I/O	I/O
V26	I/O	I/O	I/O	I/O	I/O	I/O
W1	I/O	I/O	I/O	I/O	I/O	I/O
W2	I/O	I/O	I/O	I/O	I/O	I/O
W3	I/O	I/O	I/O	I/O	I/O	I/O
W4	I/O	I/O	I/O	I/O	I/O	I/O
W5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
W22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
W23	I/O	I/O	I/O	I/O	I/O	I/O
W24	I/O	I/O	I/O	I/O	I/O	I/O
W25	I/O	I/O	I/O	I/O	I/O	I/O
W26	I/O	I/O	I/O	I/O	I/O	I/O
Y1	I/O	I/O	I/O	I/O	I/O	I/O
Y2	I/O	I/O	I/O	I/O	I/O	I/O
Y3	I/O	I/O	I/O	I/O	I/O	I/O
Y4	NC	I/O	I/O	I/O	I/O	I/O
Y5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
Y22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
Y23	NC	I/O	I/O	I/O	I/O	I/O
Y24	NC	I/O	I/O	I/O	I/O	I/O
Y25	NC	I/O	I/O	I/O	I/O	I/O
Y26	NC	I/O	I/O	I/O	I/O	I/O
AA1	I/O	I/O	I/O	I/O	I/O	I/O
AA2	NC	I/O	I/O	I/O	I/O	I/O
AA3	NC	I/O	I/O	I/O	I/O	I/O
AA4	NC	I/O	I/O	I/O	I/O	I/O
AA5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AA22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AA23	NC	I/O	I/O	I/O	I/O	I/O
AA24	NC	I/O	I/O	I/O	I/O	I/O
AA25	NC	I/O	I/O	I/O	I/O	I/O
AA26	NC	I/O	I/O	I/O	I/O	I/O
AB1	NC	I/O	I/O	I/O	I/O	I/O
AB2	NC	I/O	I/O	I/O	I/O	I/O
AB3	NC	I/O	I/O	I/O	I/O	I/O
AB4	NC	I/O	I/O	I/O	I/O	I/O
AB5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB6	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB8	I/O	I/O	I/O	I/O	I/O	I/O
AB9	I/O	I/O	I/O	I/O	I/O	I/O
AB10	I/O	I/O	I/O	I/O	I/O	I/O
AB11	I/O	I/O	I/O	I/O	I/O	I/O
AB12	I/O	I/O	I/O	I/O	I/O	I/O
AB13	I/O	I/O	I/O	I/O	I/O	I/O
AB14	I/O	I/O	I/O	I/O	I/O	I/O
AB15	I/O	I/O	I/O	I/O	I/O	I/O
AB16	I/O	I/O	I/O	I/O	I/O	I/O
AB17	I/O	I/O	I/O	I/O	I/O	I/O
AB18	I/O	I/O	I/O	I/O	I/O	I/O
AB19	I/O	I/O	I/O	I/O	I/O	I/O
AB20	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB21	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB23	NC	I/O	I/O	I/O	I/O	I/O
AB24	NC	I/O	I/O	I/O	I/O	I/O
AB25	NC	I/O	NC	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
AB26	NC	NC	I/O	I/O	I/O	I/O
AC1	NC	I/O	I/O	I/O	I/O	I/O
AC2	NC	I/O	I/O	I/O	I/O	I/O
AC3	NC	I/O	I/O	I/O	I/O	I/O
AC4	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AC5	NC	NC	I/O	I/O	I/O	I/O
AC6	I/O	I/O	I/O	I/O	I/O	I/O
AC7	I/O	I/O	I/O	I/O	I/O	I/O
AC8	I/O	I/O	I/O	I/O	I/O	I/O
AC9	I/O	I/O	I/O	I/O	I/O	I/O
AC10	I/O	I/O	I/O	I/O	I/O	I/O
AC11	I/O	I/O	I/O	I/O	I/O	I/O
AC12	I/O	I/O	I/O	I/O	I/O	I/O
AC13	I/O	I/O	I/O	I/O	I/O	I/O
AC14	I/O	I/O	I/O	I/O	I/O	I/O
AC15	I/O	I/O	I/O	I/O	I/O	I/O
AC16	I/O	I/O	I/O	I/O	I/O	I/O
AC17	I/O	I/O	I/O	I/O	I/O	I/O
AC18	I/O	I/O	I/O	I/O	I/O	I/O
AC19	I/O	I/O	I/O	I/O	I/O	I/O
AC20	I/O	I/O	I/O	I/O	I/O	I/O
AC21	TMS	TMS	TMS	TMS	TMS	TMS
AC22	TDO	TDO	TDO	TDO	TDO	TDO
AC23	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AC24	RCK	RCK	RCK	RCK	RCK	RCK
AC25	NC	NC	I/O	I/O	I/O	I/O
AC26	NC	I/O	I/O	I/O	I/O	I/O
AD1	NC	NC	NC	I/O	I/O	I/O
AD2	NC	I/O	I/O	I/O	I/O	I/O
AD3	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AD4	NC	NC	I/O	I/O	I/O	I/O
AD5	NC	NC	I/O	I/O	I/O	I/O
AD6	NC	NC	I/O	I/O	I/O	I/O
AD7	I/O	I/O	I/O	I/O	I/O	I/O
AD8	I/O	I/O	I/O	I/O	I/O	I/O
AD9	I/O	I/O	I/O	I/O	I/O	I/O
AD10	I/O	I/O	I/O	I/O	I/O	I/O
AD11	I/O	I/O	I/O	I/O	I/O	I/O
AD12	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA (Continued)

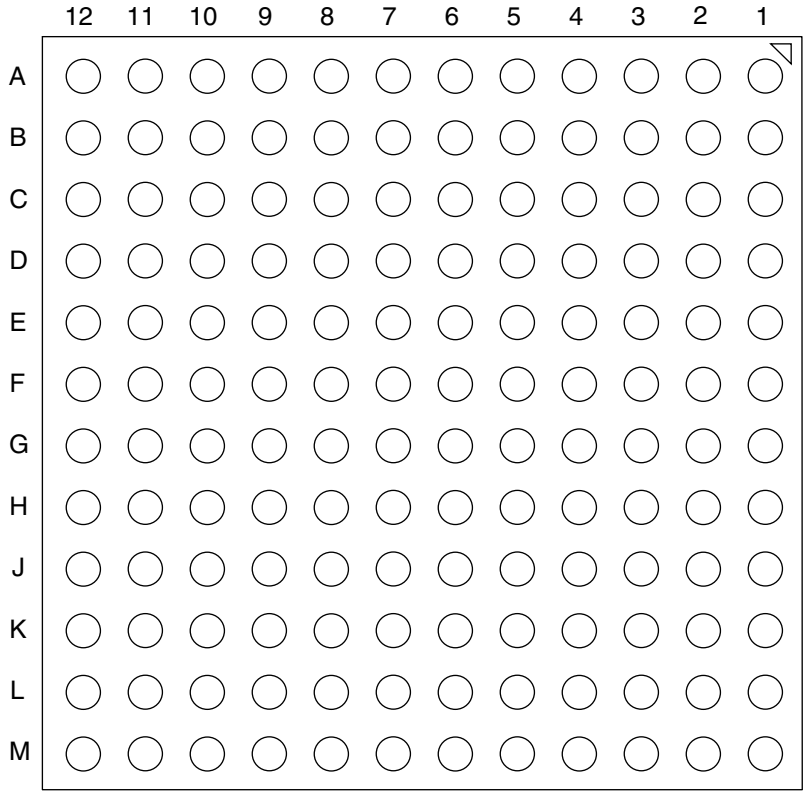
Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
AD13	I/O	I/O	I/O	I/O	I/O	I/O
AD14	I/O	I/O	I/O	I/O	I/O	I/O
AD15	I/O	I/O	I/O	I/O	I/O	I/O
AD16	I/O	I/O	I/O	I/O	I/O	I/O
AD17	I/O	I/O	I/O	I/O	I/O	I/O
AD18	I/O	I/O	I/O	I/O	I/O	I/O
AD19	I/O	I/O	I/O	I/O	I/O	I/O
AD20	NC	NC	I/O	I/O	I/O	I/O
AD21	TCK	TCK	TCK	TCK	TCK	TCK
AD22	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
AD23	NC	NC	NC	I/O	I/O	I/O
AD24	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AD25	NC	NC	I/O	I/O	I/O	I/O
AD26	NC	NC	I/O	I/O	I/O	I/O
AE1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AE2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AE3	NC	NC	I/O	I/O	I/O	I/O
AE4	NC	NC	I/O	I/O	I/O	I/O
AE5	NC	NC	I/O	I/O	I/O	I/O
AE6	NC	NC	I/O	I/O	I/O	I/O
AE7	NC	NC	I/O	I/O	I/O	I/O
AE8	I/O	I/O	I/O	I/O	I/O	I/O
AE9	I/O	I/O	I/O	I/O	I/O	I/O
AE10	I/O	I/O	I/O	I/O	I/O	I/O
AE11	I/O	I/O	I/O	I/O	I/O	I/O
AE12	I/O	I/O	I/O	I/O	I/O	I/O
AE13	I/O	I/O	I/O	I/O	I/O	I/O
AE14	I/O	I/O	I/O	I/O	I/O	I/O
AE15	I/O	I/O	I/O	I/O	I/O	I/O
AE16	I/O	I/O	I/O	I/O	I/O	I/O
AE17	I/O	I/O	I/O	I/O	I/O	I/O
AE18	I/O	I/O	I/O	I/O	I/O	I/O
AE19	I/O	I/O	I/O	I/O	I/O	I/O
AE20	NC	NC	I/O	I/O	I/O	I/O
AE21	NC	NC	I/O	I/O	I/O	I/O
AE22	NC	NC	I/O	I/O	I/O	I/O
AE23	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
AE24	TRST	TRST	TRST	TRST	TRST	TRST
AE25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

456-Pin PBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function	APA750 Function	APA1000 Function
AE26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF3	NC	NC	I/O	I/O	I/O	I/O
AF4	NC	NC	I/O	I/O	I/O	I/O
AF5	NC	NC	I/O	I/O	I/O	I/O
AF6	NC	NC	I/O	I/O	I/O	I/O
AF7	NC	NC	I/O	I/O	I/O	I/O
AF8	NC	NC	NC	I/O	I/O	I/O
AF9	I/O	I/O	I/O	I/O	I/O	I/O
AF10	I/O	I/O	I/O	I/O	I/O	I/O
AF11	I/O	I/O	I/O	I/O	I/O	I/O
AF12	I/O	I/O	I/O	I/O	I/O	I/O
AF13	I/O	I/O	I/O	I/O	I/O	I/O
AF14	I/O	I/O	I/O	I/O	I/O	I/O
AF15	I/O	I/O	I/O	I/O	I/O	I/O
AF16	I/O	I/O	I/O	I/O	I/O	I/O
AF17	I/O	I/O	I/O	I/O	I/O	I/O
AF18	NC	NC	I/O	I/O	I/O	I/O
AF19	NC	NC	I/O	I/O	I/O	I/O
AF20	NC	NC	I/O	I/O	I/O	I/O
AF21	NC	NC	I/O	I/O	I/O	I/O
AF22	NC	NC	I/O	I/O	I/O	I/O
AF23	TDI	TDI	TDI	TDI	TDI	TDI
AF24	NC	NC	I/O	I/O	I/O	I/O
AF25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

Package Assignments (Continued)

144-FBGA (Bottom View)



144-FBGA Pin

Pin Number	APA150 Function	APA300 Function	APA450 Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	GND	GND	GND
A7	I/O	I/O	I/O
A8	V_{DD}	V_{DD}	V_{DD}
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	GL	GL	GL
C3	I/O	I/O	I/O
C4	V_{DD}	V_{DD}	V_{DD}
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O

144-FBGA Pin (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	V_{DD}	V_{DD}	V_{DD}
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	V_{DDP}	V_{DDP}	V_{DDP}
E5	I/O	I/O	I/O
E6	V_{DDP}	V_{DDP}	V_{DDP}
E7	V_{DDP}	V_{DDP}	V_{DDP}
E8	AVDD	AVDD	AVDD
E9	V_{DDP}	V_{DDP}	V_{DDP}
E10	V_{DD}	V_{DD}	V_{DD}
E11	NPECL	NPECL	NPECL
E12	AGND	AGND	AGND
F1	GL	GL	GL
F2	AGND	AGND	AGND
F3	I/O	I/O	I/O
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	I/O	I/O	I/O
F9	GL	GL	GL
F10	GND	GND	GND
F11	PPECL	PPECL	PPECL
F12	GL	GL	GL
G1	PPECL	PPECL	PPECL
G2	GND	GND	GND
G3	AVDD	AVDD	AVDD
G4	NPECL	NPECL	NPECL
G5	GND	GND	GND
G6	GND	GND	GND

144-FBGA Pin (Continued)

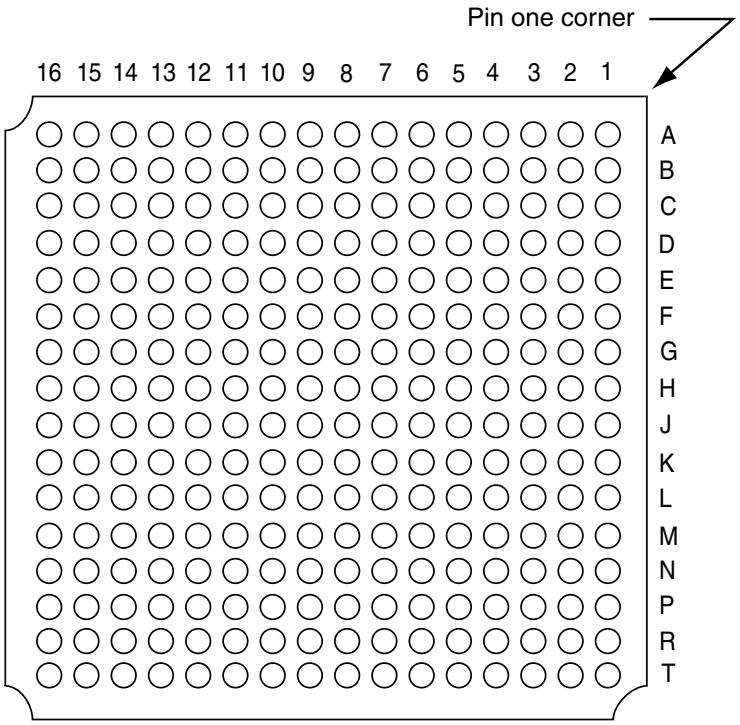
Pin Number	APA150 Function	APA300 Function	APA450 Function
G7	GND	GND	GND
G8	I/O	I/O	I/O
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	V_{DD}	V_{DD}	V_{DD}
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V_{DD}	V_{DD}	V_{DD}
H6	I/O	I/O	I/O
H7	I/O	I/O	I/O
H8	I/O	I/O	I/O
H9	I/O	I/O	I/O
H10	V_{DDP}	V_{DDP}	V_{DDP}
H11	I/O	I/O	I/O
H12	V_{DD}	V_{DD}	V_{DD}
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	V_{DDP}	V_{DDP}	V_{DDP}
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	I/O	I/O	I/O
J7	V_{DD}	V_{DD}	V_{DD}
J8	TCK	TCK	TCK
J9	I/O	I/O	I/O
J10	TDO	TDO	TDO
J11	I/O	I/O	I/O
J12	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O

144-FBGA Pin (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	V_{DDP}	V_{DDP}	V_{DDP}
L6	I/O	I/O	I/O
L7	I/O	I/O	I/O
L8	I/O	I/O	I/O
L9	TMS	TMS	TMS
L10	RCK	RCK	RCK
L11	I/O	I/O	I/O
L12	TRST	TRST	TRST
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	I/O
M8	I/O	I/O	I/O
M9	TDI	TDI	TDI
M10	V_{DDP}	V_{DDP}	V_{DDP}
M11	V_{PP}	V_{PP}	V_{PP}
M12	V_{PN}	V_{PN}	V_{PN}

Package Assignments (Continued)

256-FBGA (Bottom View)



256-Pin FBGA

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
A1	GND	GND	GND	GND
A2	I/O	I/O	I/O	I/O
A3	I/O	I/O	I/O	I/O
A4	I/O	I/O	I/O	I/O
A5	I/O	I/O	I/O	I/O
A6	I/O	I/O	I/O	I/O
A7	I/O	I/O	I/O	I/O
A8	I/O	I/O	I/O	I/O
A9	I/O	I/O	I/O	I/O
A10	I/O	I/O	I/O	I/O
A11	I/O	I/O	I/O	I/O
A12	I/O	I/O	I/O	I/O
A13	I/O	I/O	I/O	I/O
A14	I/O	I/O	I/O	I/O
A15	I/O	I/O	I/O	I/O
A16	GND	GND	GND	GND
B1	I/O	I/O	I/O	I/O
B2	I/O	I/O	I/O	I/O
B3	I/O	I/O	I/O	I/O
B4	I/O	I/O	I/O	I/O
B5	I/O	I/O	I/O	I/O
B6	I/O	I/O	I/O	I/O
B7	I/O	I/O	I/O	I/O
B8	I/O	I/O	I/O	I/O
B9	I/O	I/O	I/O	I/O
B10	I/O	I/O	I/O	I/O
B11	I/O	I/O	I/O	I/O
B12	I/O	I/O	I/O	I/O
B13	I/O	I/O	I/O	I/O
B14	I/O	I/O	I/O	I/O
B15	I/O	I/O	I/O	I/O
B16	I/O	I/O	I/O	I/O
C1	I/O	I/O	I/O	I/O
C2	I/O	I/O	I/O	I/O
C3	I/O	I/O	I/O	I/O
C4	I/O	I/O	I/O	I/O
C5	I/O	I/O	I/O	I/O
C6	I/O	I/O	I/O	I/O
C7	I/O	I/O	I/O	I/O

256-Pin FBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
C8	I/O	I/O	I/O	I/O
C9	I/O	I/O	I/O	I/O
C10	I/O	I/O	I/O	I/O
C11	I/O	I/O	I/O	I/O
C12	I/O	I/O	I/O	I/O
C13	I/O	I/O	I/O	I/O
C14	I/O	I/O	I/O	I/O
C15	I/O	I/O	I/O	I/O
C16	I/O	I/O	I/O	I/O
D1	I/O	I/O	I/O	I/O
D2	I/O	I/O	I/O	I/O
D3	I/O	I/O	I/O	I/O
D4	I/O	I/O	I/O	I/O
D5	I/O	I/O	I/O	I/O
D6	I/O	I/O	I/O	I/O
D7	I/O	I/O	I/O	I/O
D8	I/O	I/O	I/O	I/O
D9	I/O	I/O	I/O	I/O
D10	I/O	I/O	I/O	I/O
D11	I/O	I/O	I/O	I/O
D12	I/O	I/O	I/O	I/O
D13	I/O	I/O	I/O	I/O
D14	I/O	I/O	I/O	I/O
D15	I/O	I/O	I/O	I/O
D16	I/O	I/O	I/O	I/O
E1	I/O	I/O	I/O	I/O
E2	I/O	I/O	I/O	I/O
E3	I/O	I/O	I/O	I/O
E4	I/O	I/O	I/O	I/O
E5	I/O	I/O	I/O	I/O
E6	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E7	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E8	I/O	I/O	I/O	I/O
E9	I/O	I/O	I/O	I/O
E10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E11	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E12	I/O	I/O	I/O	I/O
E13	I/O	I/O	I/O	I/O
E14	I/O	I/O	I/O	I/O

256-Pin FBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
E15	I/O	I/O	I/O	I/O
E16	I/O	I/O	I/O	I/O
F1	I/O	I/O	I/O	I/O
F2	I/O	I/O	I/O	I/O
F3	I/O	I/O	I/O	I/O
F4	I/O	I/O	I/O	I/O
F5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
F6	GND	GND	GND	GND
F7	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F9	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F10	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F11	GND	GND	GND	GND
F12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
F13	I/O	I/O	I/O	I/O
F14	I/O	I/O	I/O	I/O
F15	I/O	I/O	I/O	I/O
F16	I/O	I/O	I/O	I/O
G1	I/O	I/O	I/O	I/O
G2	I/O	I/O	I/O	I/O
G3	I/O	I/O	I/O	I/O
G4	I/O	I/O	I/O	I/O
G5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
G6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G7	GND	GND	GND	GND
G8	GND	GND	GND	GND
G9	GND	GND	GND	GND
G10	GND	GND	GND	GND
G11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
G13	I/O	I/O	I/O	I/O
G14	I/O	I/O	I/O	I/O
G15	I/O	I/O	I/O	I/O
G16	I/O	I/O	I/O	I/O
H1	GL	GL	GL	GL
H2	NPECL	NPECL	NPECL	NPECL
H3	I/O	I/O	I/O	I/O
H4	AGND	AGND	AGND	AGND
H5	I/O	I/O	I/O	I/O

256-Pin FBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
H6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H7	GND	GND	GND	GND
H8	GND	GND	GND	GND
H9	GND	GND	GND	GND
H10	GND	GND	GND	GND
H11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H12	I/O	I/O	I/O	I/O
H13	I/O	I/O	I/O	I/O
H14	NPECL	NPECL	NPECL	NPECL
H15	AGND	AGND	AGND	AGND
H16	GL	GL	GL	GL
J1	GL	GL	GL	GL
J2	PPECL	PPECL	PPECL	PPECL
J3	AVDD	AVDD	AVDD	AVDD
J4	I/O	I/O	I/O	I/O
J5	I/O	I/O	I/O	I/O
J6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
J7	GND	GND	GND	GND
J8	GND	GND	GND	GND
J9	GND	GND	GND	GND
J10	GND	GND	GND	GND
J11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
J12	I/O	I/O	I/O	I/O
J13	PPECL	PPECL	PPECL	PPECL
J14	I/O	I/O	I/O	I/O
J15	AVDD	AVDD	AVDD	AVDD
J16	GL	GL	GL	GL
K1	I/O	I/O	I/O	I/O
K2	I/O	I/O	I/O	I/O
K3	I/O	I/O	I/O	I/O
K4	I/O	I/O	I/O	I/O
K5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
K6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
K7	GND	GND	GND	GND
K8	GND	GND	GND	GND
K9	GND	GND	GND	GND
K10	GND	GND	GND	GND
K11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
K12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

256-Pin FBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
K13	I/O	I/O	I/O	I/O
K14	I/O	I/O	I/O	I/O
K15	I/O	I/O	I/O	I/O
K16	I/O	I/O	I/O	I/O
L1	I/O	I/O	I/O	I/O
L2	I/O	I/O	I/O	I/O
L3	I/O	I/O	I/O	I/O
L4	I/O	I/O	I/O	I/O
L5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
L6	GND	GND	GND	GND
L7	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L9	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L10	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L11	GND	GND	GND	GND
L12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
L13	I/O	I/O	I/O	I/O
L14	I/O	I/O	I/O	I/O
L15	I/O	I/O	I/O	I/O
L16	I/O	I/O	I/O	I/O
M1	I/O	I/O	I/O	I/O
M2	I/O	I/O	I/O	I/O
M3	I/O	I/O	I/O	I/O
M4	I/O	I/O	I/O	I/O
M5	I/O	I/O	I/O	I/O
M6	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M7	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M8	I/O	I/O	I/O	I/O
M9	I/O	I/O	I/O	I/O
M10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M11	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M12	I/O	I/O	I/O	I/O
M13	I/O	I/O	I/O	I/O
M14	I/O	I/O	I/O	I/O
M15	I/O	I/O	I/O	I/O
M16	I/O	I/O	I/O	I/O
N1	I/O	I/O	I/O	I/O
N2	I/O	I/O	I/O	I/O
N3	I/O	I/O	I/O	I/O

256-Pin FBGA (Continued)

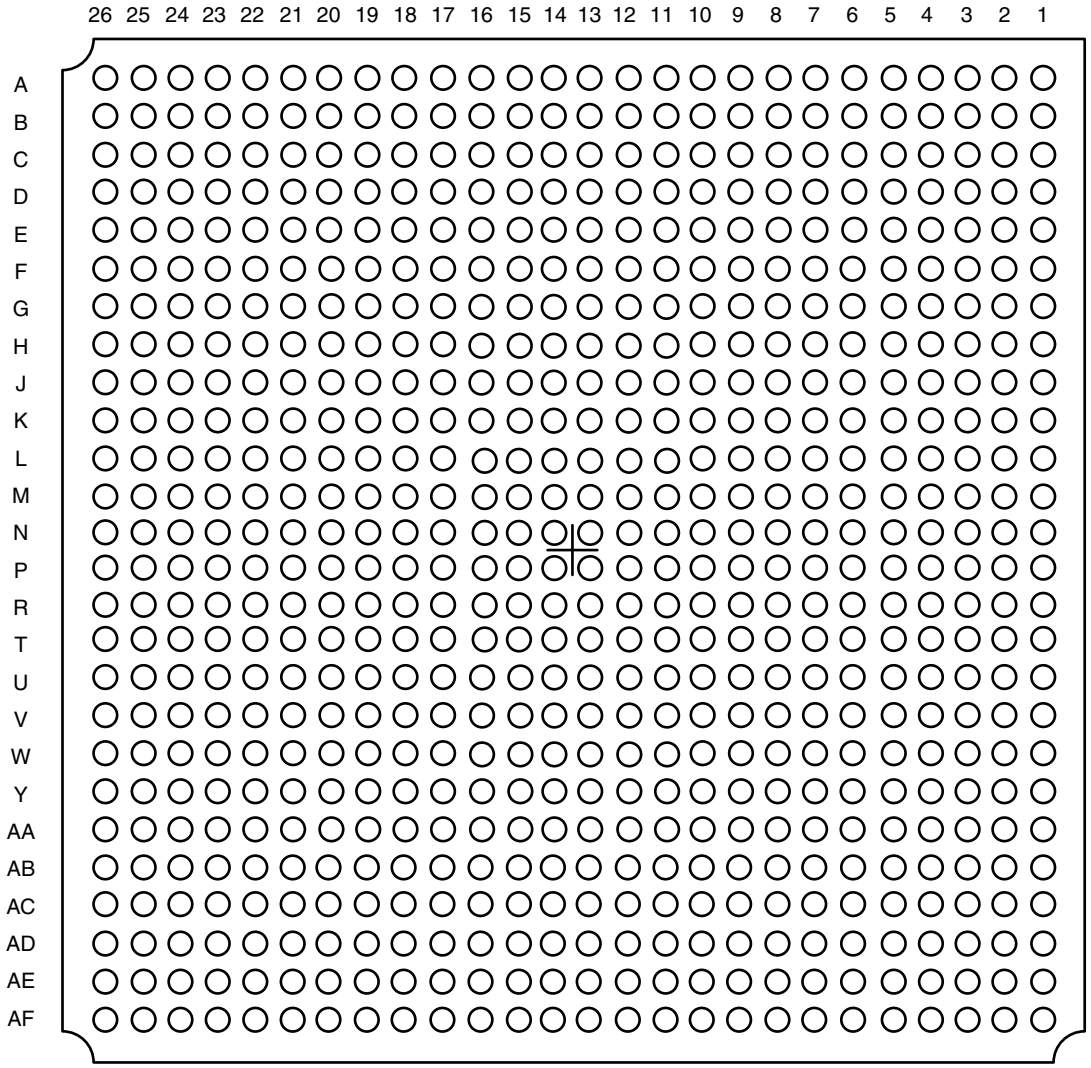
Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
N4	I/O	I/O	I/O	I/O
N5	I/O	I/O	I/O	I/O
N6	I/O	I/O	I/O	I/O
N7	I/O	I/O	I/O	I/O
N8	I/O	I/O	I/O	I/O
N9	I/O	I/O	I/O	I/O
N10	I/O	I/O	I/O	I/O
N11	I/O	I/O	I/O	I/O
N12	I/O	I/O	I/O	I/O
N13	I/O	I/O	I/O	I/O
N14	RCK	RCK	RCK	RCK
N15	I/O	I/O	I/O	I/O
N16	I/O	I/O	I/O	I/O
P1	I/O	I/O	I/O	I/O
P2	I/O	I/O	I/O	I/O
P3	I/O	I/O	I/O	I/O
P4	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O
P6	I/O	I/O	I/O	I/O
P7	I/O	I/O	I/O	I/O
P8	I/O	I/O	I/O	I/O
P9	I/O	I/O	I/O	I/O
P10	I/O	I/O	I/O	I/O
P11	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O
P13	TCK	TCK	TCK	TCK
P14	V_{PP}	V_{PP}	V_{PP}	V_{PP}
P15	TRST	TRST	TRST	TRST
P16	I/O	I/O	I/O	I/O
R1	I/O	I/O	I/O	I/O
R2	I/O	I/O	I/O	I/O
R3	I/O	I/O	I/O	I/O
R4	I/O	I/O	I/O	I/O
R5	I/O	I/O	I/O	I/O
R6	I/O	I/O	I/O	I/O
R7	I/O	I/O	I/O	I/O
R8	I/O	I/O	I/O	I/O
R9	I/O	I/O	I/O	I/O
R10	I/O	I/O	I/O	I/O

256-Pin FBGA (Continued)

Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
R11	I/O	I/O	I/O	I/O
R12	I/O	I/O	I/O	I/O
R13	I/O	I/O	I/O	I/O
R14	TDI	TDI	TDI	TDI
R15	V_{PN}	V_{PN}	V_{PN}	V_{PN}
R16	TDO	TDO	TDO	TDO
T1	GND	GND	GND	GND
T2	I/O	I/O	I/O	I/O
T3	I/O	I/O	I/O	I/O
T4	I/O	I/O	I/O	I/O
T5	I/O	I/O	I/O	I/O
T6	I/O	I/O	I/O	I/O
T7	I/O	I/O	I/O	I/O
T8	I/O	I/O	I/O	I/O
T9	I/O	I/O	I/O	I/O
T10	I/O	I/O	I/O	I/O
T11	I/O	I/O	I/O	I/O
T12	I/O	I/O	I/O	I/O
T13	I/O	I/O	I/O	I/O
T14	I/O	I/O	I/O	I/O
T15	TMS	TMS	TMS	TMS
T16	GND	GND	GND	GND

Package Pin Assignments (Continued)

676-Pin FBGA (Bottom View)



676-FBGA Pin

Pin Number	APA600 Function	APA750 Function
A1	GND	GND
A2	GND	GND
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	I/O	I/O
A22	I/O	I/O
A23	I/O	I/O
A24	I/O	I/O
A25	GND	GND
A26	GND	GND
B1	GND	GND
B2	GND	GND
B3	GND	GND
B4	GND	GND
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	I/O	I/O
B22	I/O	I/O
B23	I/O	I/O
B24	I/O	I/O
B25	GND	GND
B26	GND	GND
C1	GND	GND
C2	GND	GND
C3	GND	GND
C4	GND	GND
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	I/O	I/O
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	I/O	I/O
C26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
D1	I/O	I/O
D2	I/O	I/O
D3	GND	GND
D4	I/O	I/O
D5	I/O	I/O
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
D23	I/O	I/O
D24	I/O	I/O
D25	I/O	I/O
D26	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	I/O	I/O
E26	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	GND	GND
F6	I/O	I/O
F7	NC	NC
F8	I/O	I/O
F9	I/O	I/O
F10	I/O	I/O
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	V_{DD}	V_{DD}
G9	NC	NC
G10	I/O	I/O
G11	NC	NC
G12	I/O	I/O
G13	NC	NC
G14	I/O	I/O
G15	NC	NC
G16	I/O	I/O
G17	NC	NC
G18	I/O	I/O
G19	V_{DDP}	V_{DDP}
G20	NC	NC
G21	I/O	I/O
G22	I/O	I/O
G23	I/O	I/O
G24	I/O	I/O
G25	I/O	I/O
G26	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	V_{DDP}	V_{DDP}
H8	V_{DD}	V_{DD}
H9	V_{DDP}	V_{DDP}
H10	V_{DDP}	V_{DDP}
H11	V_{DDP}	V_{DDP}
H12	V_{DDP}	V_{DDP}
H13	V_{DDP}	V_{DDP}

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
H14	V_{DDP}	V_{DDP}
H15	V_{DDP}	V_{DDP}
H16	V_{DDP}	V_{DDP}
H17	V_{DDP}	V_{DDP}
H18	V_{DDP}	V_{DDP}
H19	V_{DD}	V_{DD}
H20	V_{DD}	V_{DD}
H21	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	I/O	I/O
H26	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	NC	NC
J8	V_{DDP}	V_{DDP}
J9	V_{DD}	V_{DD}
J10	V_{DD}	V_{DD}
J11	V_{DD}	V_{DD}
J12	V_{DD}	V_{DD}
J13	V_{DD}	V_{DD}
J14	V_{DD}	V_{DD}
J15	V_{DD}	V_{DD}
J16	V_{DD}	V_{DD}
J17	V_{DD}	V_{DD}
J18	V_{DD}	V_{DD}
J19	V_{DDP}	V_{DDP}
J20	NC	NC
J21	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	I/O	I/O
J26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	I/O	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	V_{DDP}	V_{DDP}
K9	V_{DD}	V_{DD}
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K18	V_{DD}	V_{DD}
K19	V_{DDP}	V_{DDP}
K20	I/O	I/O
K21	I/O	I/O
K22	I/O	I/O
K23	I/O	I/O
K24	I/O	I/O
K25	I/O	I/O
K26	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	NC	NC
L8	V_{DDP}	V_{DDP}
L9	V_{DD}	V_{DD}
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L18	V_{DD}	V_{DD}
L19	V_{DDP}	V_{DDP}
L20	NC	NC
L21	I/O	I/O
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	V_{DDP}	V_{DDP}
M9	V_{DD}	V_{DD}
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M18	V_{DD}	V_{DD}
M19	V_{DDP}	V_{DDP}
M20	I/O	I/O
M21	I/O	I/O
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	I/O	I/O
M26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
N1	GL	GL
N2	AGND	AGND
N3	I/O	I/O
N4	I/O	I/O
N5	NPECL	NPECL
N6	I/O	I/O
N7	NC	NC
N8	V_{DDP}	V_{DDP}
N9	V_{DD}	V_{DD}
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N18	V_{DD}	V_{DD}
N19	V_{DDP}	V_{DDP}
N20	NC	NC
N21	I/O	I/O
N22	GL	GL
N23	I/O	I/O
N24	NPECL	NPECL
N25	GL	GL
N26	I/O	I/O
P1	GL	GL
P2	AVDD	AVDD
P3	I/O	I/O
P4	I/O	I/O
P5	PPECL	PPECL
P6	I/O	I/O
P7	I/O	I/O
P8	V_{DDP}	V_{DDP}
P9	V_{DD}	V_{DD}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P18	V_{DD}	V_{DD}
P19	V_{DDP}	V_{DDP}
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	PPECL	PPECL
P25	AVDD	AVDD
P26	AGND	AGND
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	NC	NC
R8	V_{DDP}	V_{DDP}
R9	V_{DD}	V_{DD}
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R18	V_{DD}	V_{DD}
R19	V_{DDP}	V_{DDP}
R20	NC	NC
R21	I/O	I/O
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	I/O	I/O
R26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	V_{DDP}	V_{DDP}
T9	V_{DD}	V_{DD}
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T18	V_{DD}	V_{DD}
T19	V_{DDP}	V_{DDP}
T20	I/O	I/O
T21	I/O	I/O
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	I/O	I/O
T26	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	I/O	I/O
U7	NC	NC
U8	V_{DDP}	V_{DDP}
U9	V_{DD}	V_{DD}
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U18	V_{DD}	V_{DD}
U19	V_{DDP}	V_{DDP}
U20	NC	NC
U21	I/O	I/O
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	I/O	I/O
U26	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	V_{DDP}	V_{DDP}
V9	V_{DD}	V_{DD}
V10	V_{DD}	V_{DD}
V11	V_{DD}	V_{DD}
V12	V_{DD}	V_{DD}
V13	V_{DD}	V_{DD}
V14	V_{DD}	V_{DD}
V15	V_{DD}	V_{DD}
V16	V_{DD}	V_{DD}
V17	V_{DD}	V_{DD}
V18	V_{DD}	V_{DD}
V19	V_{DDP}	V_{DDP}
V20	I/O	I/O
V21	I/O	I/O
V22	I/O	I/O
V23	I/O	I/O
V24	I/O	I/O
V25	I/O	I/O
V26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	V_{DD}	V_{DD}
W8	V_{DD}	V_{DD}
W9	V_{DDP}	V_{DDP}
W10	V_{DDP}	V_{DDP}
W11	V_{DDP}	V_{DDP}
W12	V_{DDP}	V_{DDP}
W13	V_{DDP}	V_{DDP}
W14	V_{DDP}	V_{DDP}
W15	V_{DDP}	V_{DDP}
W16	V_{DDP}	V_{DDP}
W17	V_{DDP}	V_{DDP}
W18	V_{DDP}	V_{DDP}
W19	V_{DD}	V_{DD}
W20	V_{DDP}	V_{DDP}
W21	I/O	I/O
W22	I/O	I/O
W23	I/O	I/O
W24	I/O	I/O
W25	I/O	I/O
W26	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	V_{DDP}	V_{DDP}
Y9	NC	NC
Y10	I/O	I/O
Y11	NC	NC
Y12	I/O	I/O
Y13	NC	NC

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
Y14	I/O	I/O
Y15	NC	NC
Y16	I/O	I/O
Y17	NC	NC
Y18	I/O	I/O
Y19	V_{DD}	V_{DD}
Y20	V_{PP}	V_{PP}
Y21	I/O	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	I/O	I/O
Y25	I/O	I/O
Y26	I/O	I/O
AA1	I/O	I/O
AA2	I/O	I/O
AA3	I/O	I/O
AA4	I/O	I/O
AA5	I/O	I/O
AA6	GND	GND
AA7	I/O	I/O
AA8	I/O	I/O
AA9	I/O	I/O
AA10	I/O	I/O
AA11	I/O	I/O
AA12	I/O	I/O
AA13	I/O	I/O
AA14	I/O	I/O
AA15	I/O	I/O
AA16	I/O	I/O
AA17	I/O	I/O
AA18	I/O	I/O
AA19	I/O	I/O
AA20	I/O	I/O
AA21	TDO	TDO
AA22	GND	GND
AA23	GND	GND
AA24	I/O	I/O
AA25	I/O	I/O
AA26	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
AB1	I/O	I/O
AB2	I/O	I/O
AB3	I/O	I/O
AB4	I/O	I/O
AB5	I/O	I/O
AB6	GND	GND
AB7	GND	GND
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	I/O	I/O
AB13	I/O	I/O
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	I/O	I/O
AB21	TCK	TCK
AB22	TRST	TRST
AB23	I/O	I/O
AB24	I/O	I/O
AB25	I/O	I/O
AB26	I/O	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	I/O	I/O
AC5	GND	GND
AC6	I/O	I/O
AC7	I/O	I/O
AC8	I/O	I/O
AC9	GND	GND
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	I/O
AC13	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	I/O	I/O
AC21	I/O	I/O
AC22	TMS	TMS
AC23	RCK	RCK
AC24	I/O	I/O
AC25	I/O	I/O
AC26	I/O	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	I/O	I/O
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	I/O	I/O
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	I/O	I/O
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	I/O	I/O
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	TDI	TDI
AD24	V_{PN}	V_{PN}
AD25	I/O	I/O
AD26	I/O	I/O

676-FBGA Pin (Continued)

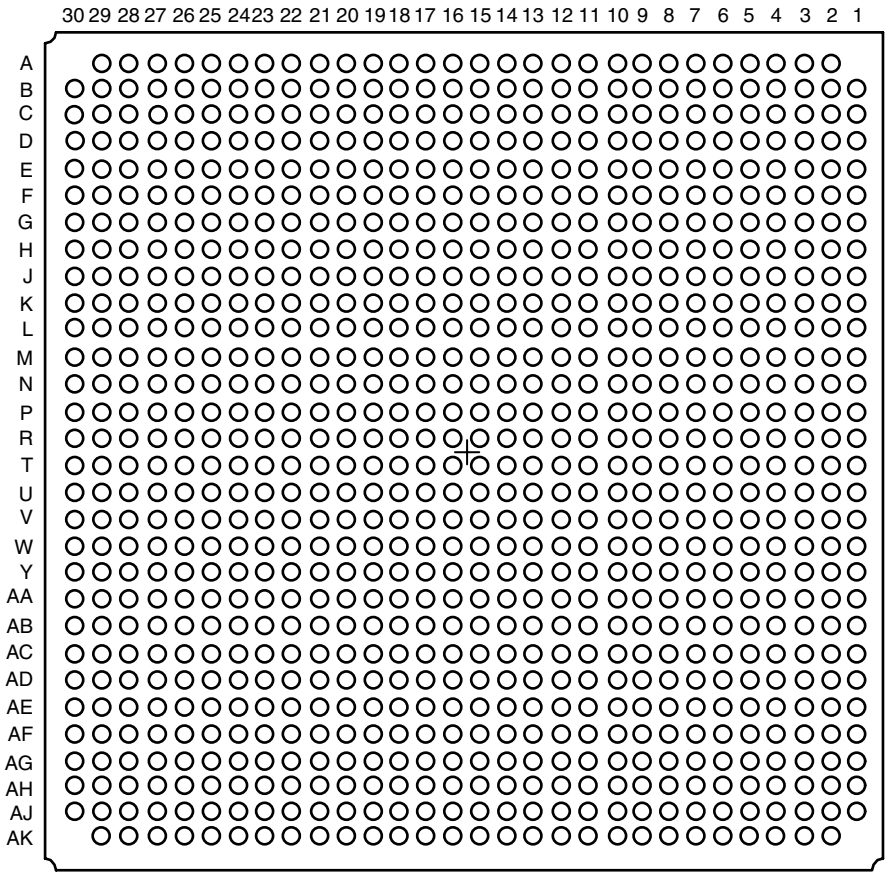
Pin Number	APA600 Function	APA750 Function
AE1	GND	GND
AE2	GND	GND
AE3	GND	GND
AE4	I/O	I/O
AE5	I/O	I/O
AE6	I/O	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	I/O	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	I/O	I/O
AE16	I/O	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	I/O	I/O
AE22	I/O	I/O
AE23	I/O	I/O
AE24	I/O	I/O
AE25	GND	GND
AE26	GND	GND
AF1	GND	GND
AF2	GND	GND
AF3	GND	GND
AF4	GND	GND
AF5	I/O	I/O
AF6	I/O	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	I/O	I/O
AF12	I/O	I/O
AF13	I/O	I/O

676-FBGA Pin (Continued)

Pin Number	APA600 Function	APA750 Function
AF14	I/O	I/O
AF15	I/O	I/O
AF16	I/O	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	I/O	I/O
AF21	I/O	I/O
AF22	I/O	I/O
AF23	I/O	I/O
AF24	I/O	I/O
AF25	GND	GND
AF26	GND	GND

Package Pin Assignments (Continued)

896-Pin FBGA (Bottom View)



896 FBGA Pin

Pin Number	APA750 Function	APA1000 Function
A2	GND	GND
A3	GND	GND
A4	I/O	I/O
A5	GND	GND
A6	I/O	I/O
A7	GND	GND
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	I/O	I/O
A22	I/O	I/O
A23	I/O	I/O
A24	GND	GND
A25	I/O	I/O
A26	GND	GND
A27	I/O	I/O
A28	GND	GND
A29	GND	GND
B1	GND	GND
B2	GND	GND
B3	I/O	I/O
B4	V_{DD}	V_{DD}
B5	I/O	I/O
B6	V_{DD}	V_{DD}
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	I/O	I/O
B22	I/O	I/O
B23	I/O	I/O
B24	I/O	I/O
B25	V_{DD}	V_{DD}
B26	I/O	I/O
B27	V_{DD}	V_{DD}
B28	I/O	I/O
B29	GND	GND
B30	GND	GND
C1	GND	GND
C2	I/O	I/O
C3	V_{DD}	V_{DD}
C4	I/O	I/O
C5	V_{DDP}	V_{DDP}
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	I/O	I/O
C26	V_{DDP}	V_{DDP}
C27	I/O	I/O
C28	V_{DD}	V_{DD}
C29	NC	I/O
C30	GND	GND
D1	I/O	I/O
D2	V_{DD}	V_{DD}
D3	I/O	I/O
D4	GND	GND
D5	I/O	I/O
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
D23	I/O	I/O
D24	I/O	I/O
D25	I/O	I/O
D26	I/O	I/O
D27	GND	GND
D28	I/O	I/O
D29	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
D30	I/O	I/O
E1	GND	GND
E2	I/O	I/O
E3	V_{DDP}	V_{DDP}
E4	I/O	I/O
E5	V_{DD}	V_{DD}
E6	I/O	I/O
E7	V_{DDP}	V_{DDP}
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	V_{DDP}	V_{DDP}
E25	I/O	I/O
E26	V_{DD}	V_{DD}
E27	I/O	I/O
E28	V_{DDP}	V_{DDP}
E29	I/O	I/O
E30	GND	GND
F1	I/O	I/O
F2	V_{DD}	V_{DD}
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F6	GND	GND
F7	I/O	I/O
F8	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
F9	I/O	I/O
F10	I/O	I/O
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	GND	GND
F26	I/O	I/O
F27	I/O	I/O
F28	I/O	I/O
F29	V_{DD}	V_{DD}
F30	I/O	I/O
G1	GND	GND
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	V_{DDP}	V_{DDP}
G6	I/O	I/O
G7	V_{DD}	V_{DD}
G8	I/O	I/O
G9	V_{DDP}	V_{DDP}
G10	I/O	I/O
G11	I/O	I/O
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
G17	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
G21	I/O	I/O
G22	V_{DDP}	V_{DDP}
G23	I/O	I/O
G24	V_{DD}	V_{DD}
G25	I/O	I/O
G26	V_{DDP}	V_{DDP}
G27	I/O	I/O
G28	I/O	I/O
G29	I/O	I/O
G30	GND	GND
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	I/O	I/O
H8	GND	GND
H9	NC	I/O
H10	NC	I/O
H11	NC	I/O
H12	NC	I/O
H13	NC	I/O
H14	NC	I/O
H15	NC	I/O
H16	NC	I/O
H17	NC	I/O
H18	NC	I/O
H19	NC	I/O
H20	NC	I/O
H21	NC	I/O
H22	NC	I/O
H23	GND	GND
H24	I/O	I/O
H25	I/O	I/O
H26	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
H27	I/O	I/O
H28	I/O	I/O
H29	I/O	I/O
H30	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	V_{DDP}	V_{DDP}
J8	I/O	I/O
J9	V_{DD}	V_{DD}
J10	NC	I/O
J11	NC	I/O
J12	NC	I/O
J13	NC	I/O
J14	NC	I/O
J15	NC	I/O
J16	NC	I/O
J17	NC	I/O
J18	NC	I/O
J19	NC	I/O
J20	NC	I/O
J21	NC	I/O
J22	V_{DD}	V_{DD}
J23	I/O	I/O
J24	V_{DDP}	V_{DDP}
J25	I/O	I/O
J26	I/O	I/O
J27	I/O	I/O
J28	I/O	I/O
J29	I/O	I/O
J30	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	I/O	I/O
K5	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
K6	I/O	I/O
K7	I/O	I/O
K8	I/O	I/O
K9	NC	I/O
K10	V_{DD}	V_{DD}
K11	NC	I/O
K12	V_{DDP}	V_{DDP}
K13	V_{DDP}	V_{DDP}
K14	V_{DDP}	V_{DDP}
K15	V_{DDP}	V_{DDP}
K16	V_{DDP}	V_{DDP}
K17	V_{DDP}	V_{DDP}
K18	V_{DDP}	V_{DDP}
K19	V_{DDP}	V_{DDP}
K20	NC	I/O
K21	V_{DD}	V_{DD}
K22	NC	I/O
K23	I/O	I/O
K24	I/O	I/O
K25	I/O	I/O
K26	I/O	I/O
K27	I/O	I/O
K28	I/O	I/O
K29	I/O	I/O
K30	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	NC	I/O
L10	NC	I/O
L11	V_{DD}	V_{DD}
L12	V_{DD}	V_{DD}
L13	V_{DD}	V_{DD}
L14	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
L15	V_{DD}	V_{DD}
L16	V_{DD}	V_{DD}
L17	V_{DD}	V_{DD}
L18	V_{DD}	V_{DD}
L19	V_{DD}	V_{DD}
L20	V_{DD}	V_{DD}
L21	NC	I/O
L22	NC	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
L27	I/O	I/O
L28	I/O	I/O
L29	I/O	I/O
L30	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	I/O	I/O
M9	NC	I/O
M10	V_{DDP}	V_{DDP}
M11	V_{DD}	V_{DD}
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M18	GND	GND
M19	GND	GND
M20	V_{DD}	V_{DD}
M21	V_{DDP}	V_{DDP}
M22	NC	I/O
M23	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
M24	I/O	I/O
M25	I/O	I/O
M26	I/O	I/O
M27	I/O	I/O
M28	I/O	I/O
M29	I/O	I/O
M30	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	I/O	I/O
N8	I/O	I/O
N9	NC	I/O
N10	V_{DDP}	V_{DDP}
N11	V_{DD}	V_{DD}
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N18	GND	GND
N19	GND	GND
N20	V_{DD}	V_{DD}
N21	V_{DDP}	V_{DDP}
N22	NC	I/O
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	I/O	I/O
N27	I/O	I/O
N28	I/O	I/O
N29	I/O	I/O
N30	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	I/O	I/O
P9	I/O	I/O
P10	V_{DDP}	V_{DDP}
P11	V_{DD}	V_{DD}
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P18	GND	GND
P19	GND	GND
P20	V_{DD}	V_{DD}
P21	V_{DDP}	V_{DDP}
P22	I/O	I/O
P23	I/O	I/O
P24	I/O	I/O
P25	I/O	I/O
P26	I/O	I/O
P27	I/O	I/O
P28	I/O	I/O
P29	I/O	I/O
P30	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	AGND	AGND
R4	NPECL	NPECL
R5	GL	GL
R6	I/O	I/O
R7	I/O	I/O
R8	I/O	I/O
R9	NC	I/O
R10	V_{DDP}	V_{DDP}
R11	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R18	GND	GND
R19	GND	GND
R20	V_{DD}	V_{DD}
R21	V_{DDP}	V_{DDP}
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	I/O	I/O
R26	I/O	I/O
R27	NPECL	NPECL
R28	AGND	AGND
R29	I/O	I/O
R30	I/O	I/O
T1	I/O	I/O
T2	AVDD	AVDD
T3	GL	GL
T4	PPECL	PPECL
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	V_{DDP}	V_{DDP}
T11	V_{DD}	V_{DD}
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T18	GND	GND
T19	GND	GND
T20	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
T21	V_{DDP}	V_{DDP}
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	I/O	I/O
T26	PPECL	PPECL
T27	GL	GL
T28	GL	GL
T29	AVDD	AVDD
T30	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	I/O	I/O
U7	I/O	I/O
U8	I/O	I/O
U9	NC	I/O
U10	V_{DDP}	V_{DDP}
U11	V_{DD}	V_{DD}
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U18	GND	GND
U19	GND	GND
U20	V_{DD}	V_{DD}
U21	V_{DDP}	V_{DDP}
U22	NC	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	I/O	I/O
U26	I/O	I/O
U27	I/O	I/O
U28	I/O	I/O
U29	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
U30	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	NC	I/O
V10	V_{DDP}	V_{DDP}
V11	V_{DD}	V_{DD}
V12	GND	GND
V13	GND	GND
V14	GND	GND
V15	GND	GND
V16	GND	GND
V17	GND	GND
V18	GND	GND
V19	GND	GND
V20	V_{DD}	V_{DD}
V21	V_{DDP}	V_{DDP}
V22	NC	I/O
V23	I/O	I/O
V24	I/O	I/O
V25	I/O	I/O
V26	I/O	I/O
V27	I/O	I/O
V28	I/O	I/O
V29	I/O	I/O
V30	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
W9	NC	I/O
W10	V_{DDP}	V_{DDP}
W11	V_{DD}	V_{DD}
W12	GND	GND
W13	GND	GND
W14	GND	GND
W15	GND	GND
W16	GND	GND
W17	GND	GND
W18	GND	GND
W19	GND	GND
W20	V_{DD}	V_{DD}
W21	V_{DDP}	V_{DDP}
W22	NC	I/O
W23	I/O	I/O
W24	I/O	I/O
W25	I/O	I/O
W26	I/O	I/O
W27	I/O	I/O
W28	I/O	I/O
W29	I/O	I/O
W30	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	I/O	I/O
Y9	NC	I/O
Y10	NC	I/O
Y11	V_{DD}	V_{DD}
Y12	V_{DD}	V_{DD}
Y13	V_{DD}	V_{DD}
Y14	V_{DD}	V_{DD}
Y15	V_{DD}	V_{DD}
Y16	V_{DD}	V_{DD}
Y17	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
Y18	V_{DD}	V_{DD}
Y19	V_{DD}	V_{DD}
Y20	V_{DD}	V_{DD}
Y21	NC	I/O
Y22	NC	I/O
Y23	I/O	I/O
Y24	I/O	I/O
Y25	I/O	I/O
Y26	I/O	I/O
Y27	I/O	I/O
Y28	I/O	I/O
Y29	I/O	I/O
Y30	I/O	I/O
AA1	I/O	I/O
AA2	I/O	I/O
AA3	I/O	I/O
AA4	I/O	I/O
AA5	I/O	I/O
AA6	I/O	I/O
AA7	I/O	I/O
AA8	I/O	I/O
AA9	NC	I/O
AA10	V_{DD}	V_{DD}
AA11	NC	I/O
AA12	V_{DDP}	V_{DDP}
AA13	V_{DDP}	V_{DDP}
AA14	V_{DDP}	V_{DDP}
AA15	V_{DDP}	V_{DDP}
AA16	V_{DDP}	V_{DDP}
AA17	V_{DDP}	V_{DDP}
AA18	V_{DDP}	V_{DDP}
AA19	V_{DDP}	V_{DDP}
AA20	NC	I/O
AA21	V_{DD}	V_{DD}
AA22	NC	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	I/O	I/O
AA26	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AA27	I/O	I/O
AA28	I/O	I/O
AA29	I/O	I/O
AA30	I/O	I/O
AB1	I/O	I/O
AB2	I/O	I/O
AB3	I/O	I/O
AB4	I/O	I/O
AB5	I/O	I/O
AB6	I/O	I/O
AB7	V_{DDP}	V_{DDP}
AB8	I/O	I/O
AB9	V_{DD}	V_{DD}
AB10	NC	I/O
AB11	NC	I/O
AB12	NC	I/O
AB13	NC	I/O
AB14	NC	I/O
AB15	NC	I/O
AB16	NC	I/O
AB17	NC	I/O
AB18	NC	I/O
AB19	NC	I/O
AB20	NC	I/O
AB21	NC	I/O
AB22	V_{DD}	V_{DD}
AB23	I/O	I/O
AB24	V_{DDP}	V_{DDP}
AB25	I/O	I/O
AB26	I/O	I/O
AB27	I/O	I/O
AB28	I/O	I/O
AB29	I/O	I/O
AB30	I/O	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	I/O	I/O
AC5	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AC6	I/O	I/O
AC7	I/O	I/O
AC8	GND	GND
AC9	NC	I/O
AC10	NC	I/O
AC11	NC	I/O
AC12	NC	I/O
AC13	NC	I/O
AC14	NC	I/O
AC15	NC	I/O
AC16	NC	I/O
AC17	NC	I/O
AC18	NC	I/O
AC19	NC	I/O
AC20	NC	I/O
AC21	NC	I/O
AC22	NC	I/O
AC23	GND	GND
AC24	I/O	I/O
AC25	I/O	I/O
AC26	I/O	I/O
AC27	I/O	I/O
AC28	I/O	I/O
AC29	I/O	I/O
AC30	I/O	I/O
AD1	GND	GND
AD2	I/O	I/O
AD3	I/O	I/O
AD4	I/O	I/O
AD5	V_{DDP}	V_{DDP}
AD6	I/O	I/O
AD7	V_{DD}	V_{DD}
AD8	I/O	I/O
AD9	V_{DDP}	V_{DDP}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	I/O	I/O
AD14	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AD15	I/O	I/O
AD16	I/O	I/O
AD17	I/O	I/O
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	V_{DDP}	V_{DDP}
AD23	TCK	TCK
AD24	V_{DD}	V_{DD}
AD25	TRST	TRST
AD26	V_{DDP}	V_{DDP}
AD27	I/O	I/O
AD28	I/O	I/O
AD29	I/O	I/O
AD30	GND	GND
AE1	I/O	I/O
AE2	V_{DD}	V_{DD}
AE3	I/O	I/O
AE4	I/O	I/O
AE5	I/O	I/O
AE6	GND	GND
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	I/O	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	I/O	I/O
AE16	I/O	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	I/O	I/O
AE22	I/O	I/O
AE23	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AE24	I/O	I/O
AE25	GND	GND
AE26	I/O	I/O
AE27	I/O	I/O
AE28	I/O	I/O
AE29	V_{DD}	V_{DD}
AE30	I/O	I/O
AF1	GND	GND
AF2	I/O	I/O
AF3	V_{DDP}	V_{DDP}
AF4	I/O	I/O
AF5	V_{DD}	V_{DD}
AF6	I/O	I/O
AF7	V_{DDP}	V_{DDP}
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	I/O	I/O
AF12	I/O	I/O
AF13	I/O	I/O
AF14	I/O	I/O
AF15	I/O	I/O
AF16	I/O	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	I/O	I/O
AF21	I/O	I/O
AF22	I/O	I/O
AF23	I/O	I/O
AF24	V_{DDP}	V_{DDP}
AF25	I/O	I/O
AF26	V_{DD}	V_{DD}
AF27	TDO	TDO
AF28	V_{DDP}	V_{DDP}
AF29	V_{PN}	V_{PN}
AF30	GND	GND
AG1	I/O	I/O
AG2	V_{DD}	V_{DD}

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AG3	I/O	I/O
AG4	GND	GND
AG5	I/O	I/O
AG6	I/O	I/O
AG7	I/O	I/O
AG8	I/O	I/O
AG9	I/O	I/O
AG10	I/O	I/O
AG11	I/O	I/O
AG12	I/O	I/O
AG13	I/O	I/O
AG14	I/O	I/O
AG15	I/O	I/O
AG16	I/O	I/O
AG17	I/O	I/O
AG18	I/O	I/O
AG19	I/O	I/O
AG20	I/O	I/O
AG21	I/O	I/O
AG22	I/O	I/O
AG23	I/O	I/O
AG24	I/O	I/O
AG25	I/O	I/O
AG26	I/O	I/O
AG27	GND	GND
AG28	RCK	RCK
AG29	V_{DD}	V_{DD}
AG30	I/O	I/O
AH1	GND	GND
AH2	I/O	I/O
AH3	V_{DD}	V_{DD}
AH4	I/O	I/O
AH5	V_{DDP}	V_{DDP}
AH6	I/O	I/O
AH7	I/O	I/O
AH8	I/O	I/O
AH9	I/O	I/O
AH10	I/O	I/O
AH11	I/O	I/O

896 FBGA Pin (Continued)

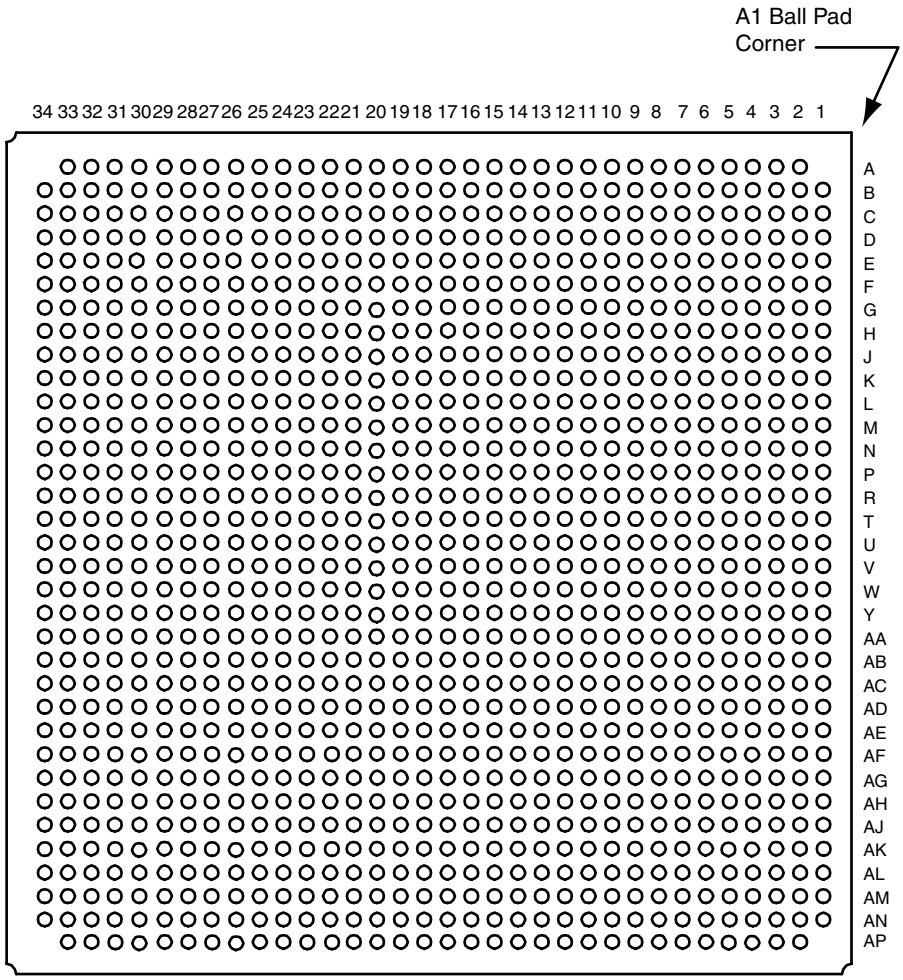
Pin Number	APA750 Function	APA1000 Function
AH12	I/O	I/O
AH13	I/O	I/O
AH14	I/O	I/O
AH15	I/O	I/O
AH16	I/O	I/O
AH17	I/O	I/O
AH18	I/O	I/O
AH19	I/O	I/O
AH20	I/O	I/O
AH21	I/O	I/O
AH22	I/O	I/O
AH23	I/O	I/O
AH24	I/O	I/O
AH25	I/O	I/O
AH26	V_{DDP}	V_{DDP}
AH27	TDI	TDI
AH28	V_{DD}	V_{DD}
AH29	V_{PP}	V_{PP}
AH30	GND	GND
AJ1	GND	GND
AJ2	GND	GND
AJ3	I/O	I/O
AJ4	V_{DD}	V_{DD}
AJ5	I/O	I/O
AJ6	V_{DD}	V_{DD}
AJ7	I/O	I/O
AJ8	I/O	I/O
AJ9	I/O	I/O
AJ10	I/O	I/O
AJ11	I/O	I/O
AJ12	I/O	I/O
AJ13	I/O	I/O
AJ14	I/O	I/O
AJ15	I/O	I/O
AJ16	I/O	I/O
AJ17	I/O	I/O
AJ18	I/O	I/O
AJ19	I/O	I/O
AJ20	I/O	I/O

896 FBGA Pin (Continued)

Pin Number	APA750 Function	APA1000 Function
AJ21	I/O	I/O
AJ22	I/O	I/O
AJ23	I/O	I/O
AJ24	I/O	I/O
AJ25	V_{DD}	V_{DD}
AJ26	I/O	I/O
AJ27	V_{DD}	V_{DD}
AJ28	TMS	TMS
AJ29	GND	GND
AJ30	GND	GND
AK2	GND	GND
AK3	GND	GND
AK4	I/O	I/O
AK5	GND	GND
AK6	I/O	I/O
AK7	GND	GND
AK8	I/O	I/O
AK9	I/O	I/O
AK10	I/O	I/O
AK11	I/O	I/O
AK12	I/O	I/O
AK13	I/O	I/O
AK14	I/O	I/O
AK15	I/O	I/O
AK16	I/O	I/O
AK17	I/O	I/O
AK18	I/O	I/O
AK19	I/O	I/O
AK20	I/O	I/O
AK21	I/O	I/O
AK22	I/O	I/O
AK23	I/O	I/O
AK24	GND	GND
AK25	I/O	I/O
AK26	GND	GND
AK27	I/O	I/O
AK28	GND	GND
AK29	GND	GND

Package Pin Assignments (Continued)

1152-Pin FBGA (Bottom View)



1152-Pin FBGA

Pin Number	APA1000 Function
A2	NC
A3	GND
A4	GND
A5	GND
A6	I/O
A7	V_{DD}
A8	V_{DD}
A9	V_{DD}
A10	V_{DD}
A11	I/O
A12	GND
A13	I/O
A14	V_{DDP}
A15	V_{DDP}
A16	I/O
A17	GND
A18	GND
A19	I/O
A20	V_{DDP}
A21	V_{DDP}
A22	I/O
A23	GND
A24	I/O
A25	V_{DD}
A26	V_{DD}
A27	V_{DD}
A28	V_{DD}
A29	I/O
A30	GND
A31	GND
A32	GND
A33	NC
B1	NC
B2	NC
B3	GND
B4	GND
B5	GND
B6	NC
B7	I/O
B8	NC
B9	I/O
B10	NC
B11	I/O
B12	GND
B13	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
B14	V_{DDP}
B15	V_{DDP}
B16	I/O
B17	GND
B18	GND
B19	I/O
B20	V_{DDP}
B21	V_{DDP}
B22	I/O
B23	GND
B24	I/O
B25	NC
B26	I/O
B27	NC
B28	I/O
B29	NC
B30	GND
B31	GND
B32	GND
B33	NC
B34	NC
C1	GND
C2	GND
C3	NC
C4	GND
C5	GND
C6	I/O
C7	GND
C8	I/O
C9	GND
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	I/O
C22	I/O
C23	I/O
C24	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
C25	I/O
C26	GND
C27	I/O
C28	GND
C29	I/O
C30	GND
C31	GND
C32	NC
C33	GND
C34	GND
D1	GND
D2	GND
D3	GND
D4	GND
D5	I/O
D6	V_{DD}
D7	I/O
D8	V_{DD}
D9	I/O
D10	I/O
D11	I/O
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
D24	I/O
D25	I/O
D26	I/O
D27	V_{DD}
D28	I/O
D29	V_{DD}
D30	I/O
D31	GND
D32	GND
D33	GND
D34	GND
E1	GND

1152-Pin FBGA

Pin Number	APA1000 Function
E2	GND
E3	GND
E4	I/O
E5	V_{DD}
E6	I/O
E7	V_{DDP}
E8	I/O
E9	I/O
E10	I/O
E11	I/O
E12	I/O
E13	I/O
E14	I/O
E15	I/O
E16	I/O
E17	I/O
E18	I/O
E19	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
E24	I/O
E25	I/O
E26	I/O
E27	I/O
E28	V_{DDP}
E29	I/O
E30	V_{DD}
E31	I/O
E32	GND
E33	GND
E34	GND
F1	I/O
F2	NC
F3	I/O
F4	V_{DD}
F5	I/O
F6	GND
F7	I/O
F8	I/O
F9	I/O
F10	I/O
F11	I/O
F12	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
F13	I/O
F14	I/O
F15	I/O
F16	I/O
F17	I/O
F18	I/O
F19	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
F24	I/O
F25	I/O
F26	I/O
F27	I/O
F28	I/O
F29	GND
F30	I/O
F31	V_{DD}
F32	I/O
F33	NC
F34	NC
G1	V_{DD}
G2	I/O
G3	GND
G4	I/O
G5	V_{DDP}
G6	I/O
G7	V_{DD}
G8	I/O
G9	V_{DDP}
G10	I/O
G11	I/O
G12	I/O
G13	I/O
G14	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
G20	I/O
G21	I/O
G22	I/O
G23	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
G24	I/O
G25	I/O
G26	V_{DDP}
G27	I/O
G28	V_{DD}
G29	I/O
G30	V_{DDP}
G31	I/O
G32	GND
G33	I/O
G34	V_{DD}
H1	V_{DD}
H2	NC
H3	I/O
H4	V_{DD}
H5	I/O
H6	I/O
H7	I/O
H8	GND
H9	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
H14	I/O
H15	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
H20	I/O
H21	I/O
H22	I/O
H23	I/O
H24	I/O
H25	I/O
H26	I/O
H27	GND
H28	I/O
H29	I/O
H30	I/O
H31	V_{DD}
H32	I/O
H33	NC
H34	V_{DD}

1152-Pin FBGA

Pin Number	APA1000 Function
J1	V_{DD}
J2	I/O
J3	GND
J4	I/O
J5	I/O
J6	I/O
J7	V_{DDP}
J8	I/O
J9	V_{DD}
J10	I/O
J11	V_{DDP}
J12	I/O
J13	I/O
J14	I/O
J15	I/O
J16	I/O
J17	I/O
J18	I/O
J19	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
J24	V_{DDP}
J25	I/O
J26	V_{DD}
J27	I/O
J28	V_{DDP}
J29	I/O
J30	I/O
J31	I/O
J32	GND
J33	I/O
J34	V_{DD}
K1	V_{DD}
K2	NC
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	I/O
K8	I/O
K9	I/O
K10	GND
K11	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
K12	I/O
K13	I/O
K14	I/O
K15	I/O
K16	I/O
K17	I/O
K18	I/O
K19	I/O
K20	I/O
K21	I/O
K22	I/O
K23	I/O
K24	I/O
K25	GND
K26	I/O
K27	I/O
K28	I/O
K29	I/O
K30	I/O
K31	I/O
K32	I/O
K33	NC
K34	V_{DD}
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	I/O
L8	I/O
L9	V_{DDP}
L10	I/O
L11	V_{DD}
L12	I/O
L13	I/O
L14	I/O
L15	I/O
L16	I/O
L17	I/O
L18	I/O
L19	I/O
L20	I/O
L21	I/O
L22	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
L23	I/O
L24	V_{DD}
L25	I/O
L26	V_{DDP}
L27	I/O
L28	I/O
L29	I/O
L30	I/O
L31	I/O
L32	I/O
L33	I/O
L34	I/O
M1	GND
M2	GND
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	I/O
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{DD}
M13	I/O
M14	V_{DDP}
M15	V_{DDP}
M16	V_{DDP}
M17	V_{DDP}
M18	V_{DDP}
M19	V_{DDP}
M20	V_{DDP}
M21	V_{DDP}
M22	I/O
M23	V_{DD}
M24	I/O
M25	I/O
M26	I/O
M27	I/O
M28	I/O
M29	I/O
M30	I/O
M31	I/O
M32	I/O
M33	GND

1152-Pin FBGA

Pin Number	APA1000 Function
M34	GND
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	I/O
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	I/O
N13	V_{DD}
N14	V_{DD}
N15	V_{DD}
N16	V_{DD}
N17	V_{DD}
N18	V_{DD}
N19	V_{DD}
N20	V_{DD}
N21	V_{DD}
N22	V_{DD}
N23	I/O
N24	I/O
N25	I/O
N26	I/O
N27	I/O
N28	I/O
N29	I/O
N30	I/O
N31	I/O
N32	I/O
N33	I/O
N34	I/O
P1	V_{DDP}
P2	V_{DDP}
P3	I/O
P4	I/O
P5	I/O
P6	I/O
P7	I/O
P8	I/O
P9	I/O
P10	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
P11	I/O
P12	V_{DDP}
P13	V_{DD}
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	GND
P21	GND
P22	V_{DD}
P23	V_{DDP}
P24	I/O
P25	I/O
P26	I/O
P27	I/O
P28	I/O
P29	I/O
P30	I/O
P31	I/O
P32	I/O
P33	V_{DDP}
P34	V_{DDP}
R1	V_{DDP}
R2	V_{DDP}
R3	I/O
R4	I/O
R5	I/O
R6	I/O
R7	I/O
R8	I/O
R9	I/O
R10	I/O
R11	I/O
R12	V_{DDP}
R13	V_{DD}
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	GND
R21	GND

1152-Pin FBGA

Pin Number	APA1000 Function
R22	V_{DD}
R23	V_{DDP}
R24	I/O
R25	I/O
R26	I/O
R27	I/O
R28	I/O
R29	I/O
R30	I/O
R31	I/O
R32	I/O
R33	V_{DDP}
R34	V_{DDP}
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T5	I/O
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	I/O
T11	I/O
T12	V_{DDP}
T13	V_{DD}
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	GND
T21	GND
T22	V_{DD}
T23	V_{DDP}
T24	I/O
T25	I/O
T26	I/O
T27	I/O
T28	I/O
T29	I/O
T30	I/O
T31	I/O
T32	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
T33	I/O
T34	I/O
U1	GND
U2	GND
U3	I/O
U4	I/O
U5	AGND
U6	NPECL
U7	GL
U8	I/O
U9	I/O
U10	I/O
U11	I/O
U12	V_{DDP}
U13	V_{DD}
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	GND
U21	GND
U22	V_{DD}
U23	V_{DDP}
U24	I/O
U25	I/O
U26	I/O
U27	I/O
U28	I/O
U29	NPECL
U30	AGND
U31	I/O
U32	I/O
U33	GND
U34	GND
V1	GND
V2	GND
V3	I/O
V4	AVDD
V5	GL
V6	PPECL
V7	I/O
V8	I/O
V9	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
V10	I/O
V11	I/O
V12	V_{DDP}
V13	V_{DD}
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	GND
V21	GND
V22	V_{DD}
V23	V_{DDP}
V24	I/O
V25	I/O
V26	I/O
V27	I/O
V28	PPECL
V29	GL
V30	GL
V31	AVDD
V32	I/O
V33	GND
V34	GND
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W5	I/O
W6	I/O
W7	I/O
W8	I/O
W9	I/O
W10	I/O
W11	I/O
W12	V_{DDP}
W13	V_{DD}
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W20	GND

1152-Pin FBGA

Pin Number	APA1000 Function
W21	GND
W22	V_{DD}
W23	V_{DDP}
W24	I/O
W25	I/O
W26	I/O
W27	I/O
W28	I/O
W29	I/O
W30	I/O
W31	I/O
W32	I/O
W33	I/O
W34	I/O
Y1	V_{DDP}
Y2	V_{DDP}
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{DDP}
Y13	V_{DD}
Y14	GND
Y15	GND
Y16	GND
Y17	GND
Y18	GND
Y19	GND
Y20	GND
Y21	GND
Y22	V_{DD}
Y23	V_{DDP}
Y24	I/O
Y25	I/O
Y26	I/O
Y27	I/O
Y28	I/O
Y29	I/O
Y30	I/O
Y31	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
Y32	I/O
Y33	V_{DDP}
Y34	V_{DDP}
AA1	V_{DDP}
AA2	V_{DDP}
AA3	I/O
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	V_{DDP}
AA13	V_{DD}
AA14	GND
AA15	GND
AA16	GND
AA17	GND
AA18	GND
AA19	GND
AA20	GND
AA21	GND
AA22	V_{DD}
AA23	V_{DDP}
AA24	I/O
AA25	I/O
AA26	I/O
AA27	I/O
AA28	I/O
AA29	I/O
AA30	I/O
AA31	I/O
AA32	I/O
AA33	V_{DDP}
AA34	V_{DDP}
AB1	I/O
AB2	I/O
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AB9	I/O
AB10	I/O
AB11	I/O
AB12	I/O
AB13	V_{DD}
AB14	V_{DD}
AB15	V_{DD}
AB16	V_{DD}
AB17	V_{DD}
AB18	V_{DD}
AB19	V_{DD}
AB20	V_{DD}
AB21	V_{DD}
AB22	V_{DD}
AB23	I/O
AB24	I/O
AB25	I/O
AB26	I/O
AB27	I/O
AB28	I/O
AB29	I/O
AB30	I/O
AB31	I/O
AB32	I/O
AB33	I/O
AB34	I/O
AC1	GND
AC2	GND
AC3	I/O
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	I/O
AC10	I/O
AC11	I/O
AC12	V_{DD}
AC13	I/O
AC14	V_{DDP}
AC15	V_{DDP}
AC16	V_{DDP}
AC17	V_{DDP}
AC18	V_{DDP}
AC19	V_{DDP}

1152-Pin FBGA

Pin Number	APA1000 Function
AC20	V_{DDP}
AC21	V_{DDP}
AC22	I/O
AC23	V_{DD}
AC24	I/O
AC25	I/O
AC26	I/O
AC27	I/O
AC28	I/O
AC29	I/O
AC30	I/O
AC31	I/O
AC32	I/O
AC33	GND
AC34	GND
AD1	I/O
AD2	I/O
AD3	I/O
AD4	I/O
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	V_{DDP}
AD10	I/O
AD11	V_{DD}
AD12	I/O
AD13	I/O
AD14	I/O
AD15	I/O
AD16	I/O
AD17	I/O
AD18	I/O
AD19	I/O
AD20	I/O
AD21	I/O
AD22	I/O
AD23	I/O
AD24	V_{DD}
AD25	I/O
AD26	V_{DDP}
AD27	I/O
AD28	I/O
AD29	I/O
AD30	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AD31	I/O
AD32	I/O
AD33	I/O
AD34	I/O
AE1	V_{DD}
AE2	NC
AE3	I/O
AE4	I/O
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	GND
AE11	I/O
AE12	I/O
AE13	I/O
AE14	I/O
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	I/O
AE23	I/O
AE24	I/O
AE25	GND
AE26	I/O
AE27	I/O
AE28	I/O
AE29	I/O
AE30	I/O
AE31	I/O
AE32	I/O
AE33	NC
AE34	V_{DD}
AF1	V_{DD}
AF2	I/O
AF3	GND
AF4	I/O
AF5	I/O
AF6	I/O
AF7	V_{DDP}

1152-Pin FBGA

Pin Number	APA1000 Function
AF8	I/O
AF9	V_{DD}
AF10	I/O
AF11	V_{DDP}
AF12	I/O
AF13	I/O
AF14	I/O
AF15	I/O
AF16	I/O
AF17	I/O
AF18	I/O
AF19	I/O
AF20	I/O
AF21	I/O
AF22	I/O
AF23	I/O
AF24	V_{DDP}
AF25	TCK
AF26	V_{DD}
AF27	TRST
AF28	V_{DDP}
AF29	I/O
AF30	I/O
AF31	I/O
AF32	GND
AF33	I/O
AF34	V_{DD}
AG1	V_{DD}
AG2	NC
AG3	I/O
AG4	V_{DD}
AG5	I/O
AG6	I/O
AG7	I/O
AG8	GND
AG9	I/O
AG10	I/O
AG11	I/O
AG12	I/O
AG13	I/O
AG14	I/O
AG15	I/O
AG16	I/O
AG17	I/O
AG18	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AG19	I/O
AG20	I/O
AG21	I/O
AG22	I/O
AG23	I/O
AG24	I/O
AG25	I/O
AG26	I/O
AG27	GND
AG28	I/O
AG29	I/O
AG30	I/O
AG31	V_{DD}
AG32	I/O
AG33	NC
AG34	V_{DD}
AH1	V_{DD}
AH2	I/O
AH3	GND
AH4	I/O
AH5	V_{DDP}
AH6	I/O
AH7	V_{DD}
AH8	I/O
AH9	V_{DDP}
AH10	I/O
AH11	I/O
AH12	I/O
AH13	I/O
AH14	I/O
AH15	I/O
AH16	I/O
AH17	I/O
AH18	I/O
AH19	I/O
AH20	I/O
AH21	I/O
AH22	I/O
AH23	I/O
AH24	I/O
AH25	I/O
AH26	V_{DDP}
AH27	I/O
AH28	V_{DD}
AH29	TDO

1152-Pin FBGA

Pin Number	APA1000 Function
AH30	V_{DDP}
AH31	VPN
AH32	GND
AH33	I/O
AH34	V_{DD}
AJ1	I/O
AJ2	NC
AJ3	I/O
AJ4	V_{DD}
AJ5	I/O
AJ6	GND
AJ7	I/O
AJ8	I/O
AJ9	I/O
AJ10	I/O
AJ11	I/O
AJ12	I/O
AJ13	I/O
AJ14	I/O
AJ15	I/O
AJ16	I/O
AJ17	I/O
AJ18	I/O
AJ19	I/O
AJ20	I/O
AJ21	I/O
AJ22	I/O
AJ23	I/O
AJ24	I/O
AJ25	I/O
AJ26	I/O
AJ27	I/O
AJ28	I/O
AJ29	GND
AJ30	RCK
AJ31	V_{DD}
AJ32	I/O
AJ33	NC
AJ34	NC
AK1	GND
AK2	GND
AK3	GND
AK4	I/O
AK5	V_{DD}
AK6	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AK7	V_{DDP}
AK8	I/O
AK9	I/O
AK10	I/O
AK11	I/O
AK12	I/O
AK13	I/O
AK14	I/O
AK15	I/O
AK16	I/O
AK17	I/O
AK18	I/O
AK19	I/O
AK20	I/O
AK21	I/O
AK22	I/O
AK23	I/O
AK24	I/O
AK25	I/O
AK26	I/O
AK27	I/O
AK28	V_{DDP}
AK29	TDI
AK30	V_{DD}
AK31	VPP
AK32	GND
AK33	GND
AK34	GND
AL1	GND
AL2	GND
AL3	GND
AL4	GND
AL5	I/O
AL6	V_{DD}
AL7	I/O
AL8	V_{DD}
AL9	I/O
AL10	I/O
AL11	I/O
AL12	I/O
AL13	I/O
AL14	I/O
AL15	I/O
AL16	I/O
AL17	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AL18	I/O
AL19	I/O
AL20	I/O
AL21	I/O
AL22	I/O
AL23	I/O
AL24	I/O
AL25	I/O
AL26	I/O
AL27	V_{DD}
AL28	I/O
AL29	V_{DD}
AL30	TMS
AL31	GND
AL32	GND
AL33	GND
AL34	GND
AM1	GND
AM2	GND
AM3	NC
AM4	GND
AM5	GND
AM6	I/O
AM7	GND
AM8	I/O
AM9	GND
AM10	I/O
AM11	I/O
AM12	I/O
AM13	I/O
AM14	I/O
AM15	I/O
AM16	I/O
AM17	I/O
AM18	I/O
AM19	I/O
AM20	I/O
AM21	I/O
AM22	I/O
AM23	I/O
AM24	I/O
AM25	I/O
AM26	GND
AM27	I/O
AM28	GND

1152-Pin FBGA

Pin Number	APA1000 Function
AM29	I/O
AM30	GND
AM31	GND
AM32	NC
AM33	GND
AM34	GND
AN1	NC
AN2	NC
AN3	GND
AN4	GND
AN5	GND
AN6	NC
AN7	I/O
AN8	NC
AN9	I/O
AN10	NC
AN11	I/O
AN12	GND
AN13	I/O
AN14	V_{DDP}
AN15	V_{DDP}
AN16	I/O
AN17	GND
AN18	GND
AN19	I/O
AN20	V_{DDP}
AN21	V_{DDP}
AN22	I/O
AN23	GND
AN24	I/O
AN25	NC
AN26	I/O
AN27	NC
AN28	I/O
AN29	NC
AN30	GND
AN31	GND
AN32	GND
AN33	NC
AN34	NC
AP2	NC
AP3	GND
AP4	GND
AP5	GND
AP6	I/O

1152-Pin FBGA

Pin Number	APA1000 Function
AP7	V_{DD}
AP8	V_{DD}
AP9	V_{DD}
AP10	V_{DD}
AP11	I/O
AP12	GND
AP13	I/O
AP14	V_{DDP}
AP15	V_{DDP}
AP16	I/O
AP17	GND
AP18	GND
AP19	I/O
AP20	V_{DDP}
AP21	V_{DDP}
AP22	I/O
AP23	GND
AP24	I/O
AP25	V_{DD}
AP26	V_{DD}
AP27	V_{DD}
AP28	V_{DD}
AP29	I/O
AP30	GND
AP31	GND
AP32	GND
AP33	NC

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (Advanced v0.6)	Page
Advanced v0.5	The description for the V_{PN} pin has changed.	page 54
Advanced v0.4	The "Plastic Device Resources" table on page 4 has been updated.	page 4
	Figure 19 and Figure 20 on page 28 have been updated.	page 28
	The "Tristate Buffer Delays" table on page 30 has been updated.	page 30
	The "Output Buffer Delays" table on page 31 has been updated.	page 31
	The "Input Buffer Delays" table on page 32 has been updated.	page 32
	The "Global Input Buffer Delays" table on page 32 has been updated.	page 32
	The "456-Pin PBGA" table on page 63 has been updated.	page 63
	The "676-FBGA Pin" table on page 87 has been updated.	page 87
Advanced v0.3	The "ProASIC PLUS Product Profile" section on page 1 has been changed.	page 1
	The "Plastic Device Resources" section on page 4 has been updated.	page 4
	The Supply Voltages table on page 10 has been updated.	page 10
	WDATA has ben changed to DI, and RDATA has been changed to DO to make them consistent with the signal names found in the *Macro Library Guide*.	
	Figure 13 on page 15 and Figure 14 on page 16 have been updated.	page 15 and page 16
	The "Design Environment" section on page 17 and Figure 18 on page 18 have been updated.	page 17 and page 18
	The table in the "Package Thermal Characteristics" section on page 19 has been updated.	page 19
	The "Calculating Power Dissipation" section on page 20 is new.	page 20
	The "Programming and Storage Temperature Limits" section on page 22 is new.	page 22
	The "Supply Voltages" section on page 22 has been updated.	page 22
	The "DC Electrical Specifications (V_{DDP} = 2.5V +/-0.2V)" section on page 23 was updated.	page 23
	The "DC Electrical Specifications (V_{DDP} = 3.3V +/-0.3V and VDD 2.5+/-0.2V)" section on page 24 was updated.	page 24
	The "AC Specifications (3.3V PCI Revision 2.2 Operation)" section on page 26 was updated.	page 26
	The "Clock Conditioning Circuit" section on page 27 was updated.	page 27
	Figure 19 on page 28 was updated.	page 28
	Figure 20 on page 28 is new.	page 28
	Tables 5, 6, and 7 from Advanced v0.3 were removed.	
	The "Memory Block SRAM Interface Signals" section on page 35 was updated.	page 35
	The "Memory Block FIFO Interface Signals" section on page 46 was updated.	page 46
	All pinout tables have been updated, and several packages are new: 208-Pin PQFP – APA150, APA300, APA450, APA600 456-Pin PBGA – APA150, APA300, APA450, APA600 144-Pin FBGA – APA150, APA300, APA450 256-Pin FBGA – APA150, APA300, APA450, APA600 676-Pin FBGA – APA600	
Advanced v0.1	Figure 15 on page 16 has been updated	page 16

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. Product Briefs are modified versions of data sheets. Data sheets are marked as "Advanced," "Preliminary," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a modified version of an Advanced data sheet containing general product information. This brief summarizes specific device and family information for non-release products.

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The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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http://www.actel.com

Actel Europe Ltd.
Maxfli Court, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Tel: +44 (0)1276 401450
Fax: +44 (0)1276 401490

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Tel: (408) 739-1010
Fax: (408) 739-1540

Actel Asia-Pacific
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Tel: +81 03-3445-7671
Fax: +81 03-3445-7668

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